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MODULAR MULTI-FUNCTION MULTI-BAND AIRBORNE RADIO SYSTEM (MFBARS)

Volume I - Executive Summary

ITT Avionics Division
390 Washington Avenue
Nutley, New Jersey 07110

October 1981

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Avionics Laboratory
Air Force Wright Aeronautical Laboratories
Air Force Systems Command
Wright-Patterson AFB, Ohio 45433

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Darlow G. Botha

DARLOW G. BOTHA
PROJECT ENGINEER
AFWAL/AAAD

C. R. Register

CHARLES R. REGISTER, Major, USAF
Acting Chief, Info Transmission Br
Avionics Laboratory

FOR THE COMMANDER

Richard H. Boivin

RICHARD H. BOIVIN, Colonel, USAF
Chief, System Avionics Division
Avionics Laboratory

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ATF
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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the results of the first two phases of the MFBARS radio architecture study. This study was aimed at establishing a cost effective and volume-conserving method of integrating tactical CNI avionics equipments. The goal was innovative integration of these systems, by a method which would allow the incorporation of new capabilities and which would take advantage of technological advances, both in-hand and projected within the near-term future (1985). Such integration is needed to reduce spiraling

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20. ABSTRACT (cont.)

life cycle costs and to alleviate severe hardware space limitation problems in tactical aircraft.

During Phase I, a set of viable MFBARS candidate architectures was developed, together with a cost evaluation of these with respect to a government-provided baseline of existing equipment, to allow meaningful comparisons.

The three MFBARS architectures proposed during Phase I were keyed to a reasonable expectation of techniques and devices projected to be available when MFBARS advanced development would be initiated in the mid '80's. The three architectures provided a graduated increase in payoff potential with associated increases in technical risk.

The Government then selected the most advanced of the three Phase I candidate system architectures for more detailed study.

During Phase II, ITT conducted a top-down, system-oriented study of the selected system approach. System configuration details and performance parameters were refined. In addition, to minimize system development risk and to provide guidance on the best direction along which MFBARS should proceed, recommended plans were defined for development of the system and supporting technology.

The main emphasis of this report is on the final recommended system configuration and associated performance parameters and recommended development plans.

19. KEY WORDS (con't.)

WBATF
Narrowband Agile Transversal Filter
NBATF
JTIDS
GPS
GPS/JTIDS
Integrated GPS/JTIDS
Integrated GPS/JTIDS/INS
SEEK TALK
AFSATCOM

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EXECUTIVE SUMMARY

1. INTRODUCTION

This report describes the results of the first two phases of the Modular Multi-function Multi-band Airborne Radio System (MFBARS) radio architecture study. This study identifies cost effective and volume-conserving methods of integrating tactical Communication, Navigation and Identification (CNI) avionics equipments for the signals shown in Figure 1.

The study goal was to develop concepts for innovative integration of these equipments by methods which would allow the incorporation of new capabilities, and which would take advantage of technological advances, both in-hand and projected to be available within the near-term future (1985). Such integration is needed to reduce spiraling life cycle costs and to alleviate a severe space problem in tactical aircraft.

1.1 STUDY OBJECTIVES

The primary objectives of the MFBARS study were to define smaller and more cost effective CNI avionics through an architecture characterized by standardization of common functional modules and interfaces designed to provide:

- reduced proliferation of unique modules
- the ability to configure, from a set of common modules, a given total CNI capability on specific platforms for a given mission
- the ability to take advantage of technological advances to improve specific common modules with a minimum of retrofit/transition cost
- the ability to incorporate new capabilities
- improved reliability with graceful degradation
- redundancy of critical functions

In meeting these objectives, it was necessary to comply with two overriding Government-imposed guidelines:

- performance standards (of each individual radio function) must be maintained or could be improved, but could not be degraded.
- signal-in-space waveforms (of each individual radio function) could not be modified.

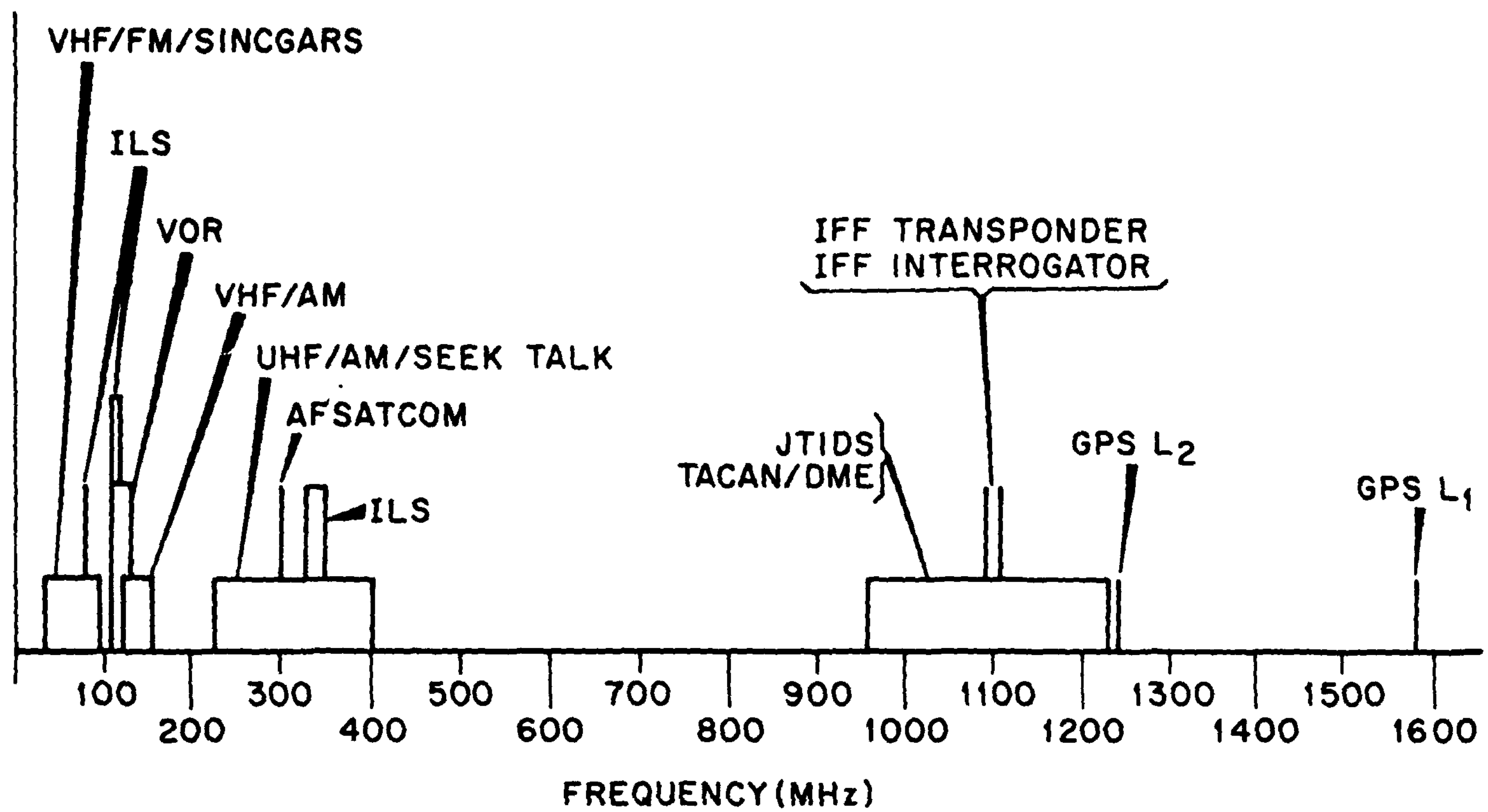


Figure 1. MFBARS CNI signals (HF not shown)

In addition, the Government directed that MFBARS designs should incorporate technology as projected to be available in 1985, the planned start of hardware development. This was done to avoid constraining MFBARS designs by technology which would be seven years old by the time hardware development started.

Finally, MFBARS interfaces with other aircraft systems were to maximize use of other standard avionics equipment, both in-being and under development as standard avionics modules. For example, all MFBARS digital interface with cockpit controls and displays would utilize DAIS. The controls and displays themselves would be standard DAIS-compatible controls and displays, not special items developed as part of the MFBARS design effort.

1.2 STUDY APPROACH

Phase I of the MFBARS study addressed broad conceptual issues of MFBARS design. Three specific candidate system architectures were defined, each with a different degree of technical risk and associated projected payoff in terms of reduced size and cost and improved operational flexibility. Each Phase I MFBARS candidate system architecture had to be functionally equivalent to a Government supplied CNI radio baseline. Realistically achievable packaging improvements were estimated for the baseline CNI radios so that physical comparisons with MFBARS designs would be fair. Tables 1,2 and 3 summarize the Phase I baseline.

It was clear from the onset of Phase I that MFBARS would confront multiple complex issues, and that it would dilute the current effort to attempt to address all of the issues, assuming that all could be identified. The study concentrated, therefore, on the areas that promised the highest payoffs. In doing this, a system-oriented top-down study approach was utilized.

The study started with an analysis of operational and mission requirements. This analysis showed that no more than 4-6 VHF/UHF radio functions were ever used simultaneously (of up to 14 VHF/UHF radios carried). This meant that considerable systems savings could be achieved by integrating VHF/UHF RF front end modules, and by adding software-controlled flexible switching and signal processing capabilities.

Similar analysis of the L-band radio functions led to the conclusion that software-controlled high speed time sharing would provide the best approach to meeting MFBARS objectives for L-band signals.

TABLE 1. BASELINE CNI RADIO FUNCTIONS

Radio	Band; Type	Phase I	Phase II
ARC 112	HF; Comm	X	
ARC 131	Low VHF, FM; Comm (30-88 MHz)	X	X
ARC 115	High VHF, AM/FM; Comm (108-156 MHz)	X	X
ARC 164	UHF,AM; Comm	X	X
ARN 118	L-Band; TACAN	X	X
APX 76	L-Band; IFF Interrogator	X	X
APX 101	L-Band; IFF Transponder	X	X
JTIDS	L-Band; Spread Spectrum Comm/Nav	X	X
GPS	L-Band; Spread Spectrum Nav	X	X
SEEK TALK	UHF Spread; Spectrum Comm	X	X
SINCGARS	VHF; Freq. Hop Comm		(some platforms)
AFSATCOM	UHF; Satellite Comm		(some platforms)

TABLE 2. MFBARS RADIO SPECTRAL REQUIREMENTS

RECEIVE:

VHF/UHF:		Freq. MHz	Modulation	Baseline Equivalent
1. VHF LO-Band Comm/Homing	Tunable/Freq. Hopped	30-88	FM	ARC-131
2. VHF LO-Band Guard	Fixed	40.5	FM	
3. VHF LO-Band Marker Beacon	Fixed	75.0	AM	
4. VHF HI-Band Localizer	Tunable	108-112	AM	ARC-108
5. VHF HI-Band VOR	Tunable	112-118	AM	
6. UHF Glide Slope	Tunable	329-335	AM	
7. VHF HI-Band Comm/ADF	Tunable	108-156	AM	ARC-115
8. VHF HI-Band Guard	Fixed	121.5	AM	
9. UHF Comm/ADF	Tunable	225-400	AM	ARC-164
10. UHF Guard	Fixed	243	AM	
11. UHF SEEK TALK	Direct Seq. PN	225-400	PN	SEEK TALK
12. UHF AFSATCOM (a)	Freq. Hopped	225-400	FSK	AFSATCOM
L-Band:				
13. JTIDS Comm/Nav	Freq. & Time Hopped & Dir. Seq. PN	960-1215	PN,PULSE	(b)
14. IFF	Fixed	1030/1090	PPM	APX-76/APX-101
15. TACAN	Tunable	960-1215	PULSE	ARN 118
16. GPS	Fixed	1227/1575	PN	(c)
17. SINCGARS (a)	Freq. Hopped	30-88		SINCGARS-V

TRANSMIT:

VHF/UHF:		Freq. MHz	Modulation	Power (Watts)	Baseline Equivalent
1. VHF LO-Band Comm	Tunable/Freq. Hopped	30-88	FM	10/1	ARC-131
2. VHF HI-Band Comm	Tunable	118-156	AM	10	ARC-115
3. UHF Comm	Tunable	225-400	AM	10	ARC-164
4. UHF SEEK TALK	Direct Seq. PN	225-400	PN	10	SEEK TALK
5. AFSATCOM (a)	Freq. Hopped	225-400	FSK	40	AFSATCOM
L-Band:					
6. JTIDS Comm/Nav	Freq. & Time Hopped & Dir. Seq. PN	960-1215	PN,Pulse	200/1000	(b)
7. TACAN	Tunable	960-1215	Pulse	1000	ARN-118
8. IFF	Fixed	1030/1090	PPM	500	APX-76/APX-101
9. SINCGARS (a)	Freq. Hopped	30-88			SINCGAR V

(a) Some platforms only
(b) ATDMA/TDMA or DTDMA/TDMA, to be determined by Government
(c) Improved X-set

TABLE 3. FUNCTIONAL REQUIREMENTS

VHF/UHF Communications

- Up to three simultaneous receive voice channels, including one guard channel.
- Transmission on one channel at a time (dual VHF/UHF transmitters provide redundancy, but only one transmits at a time).
- Transmit and receive capability in each of the bands: 30-88 MHz, 108-156 MHz, and 225-400 MHz.
- 25 kHz channel separation.
- Ability to pre-program channels and processors.
- Ability to pre-program information transfer functions.
- SEEK TALK spread spectrum voice capability.
- AFSATCOM low data rate capability.
- SINCGARS-V frequency hopping voice capability.

L-Band Communications

- JTIDS ATDMA/TDMA or DTDMA/TDMA (8 simultaneous channels for worst case ATDMA/TDMA acquisition and sync; 4 channels adequate for DTDMA/TDMA).

Navigation and IFF (VHF/UHF and L-band)

- ILS/VOR: Marker beacon, localizer, glide slope, VOR
- GPS: Precision navigation.
- TACAN: Air-to-ground and air-to-air; receive and transmit.
- JTIDS: Relative navigation; receive and transmit.
- IFF: Transponder and interrogator; all modes including Mark XII; receive and transmit.
- VHF FM: Homing (back-up nav).
- VHF AM: ADF (back-up nav).
- UHF AM: ADF (back-up nav).

Analysis of HF radio functions led to the conclusion that only marginal (approximately 5 percent) savings would be realized by integration of HF radio functions. Furthermore, tactical mission use of HF is very limited. Therefore, unless new factors (such as widespread introduction of new adaptive HF techniques) were considered, it would not be cost effective to integrate HF with the other radio functions. The resultant design approaches, therefore, consider HF as a non-integrated CNI function.

In addition to identification of flexible switching (for VHF/UHF bands) and high speed time sharing (for L-band) as candidate techniques for CNI radio integration, cost analyses were performed for generic radio sets. It was revealed that more than 50 percent of their cost is commonly contained in the RF circuitry. One focus of the study was therefore concentrated in the reduction of or simplification of the many RF components and related RF signal processing circuits. Common RF modules and other potential RF cost saving approaches were identified and evaluated. Promising cost effective design approaches were incorporated in candidate designs.

At the end of Phase I, comparisons were made of each candidate system architecture against the baseline. Phase II of the study then went into greater design depth for one of the architectures, as described below. A slightly modified baseline was defined for Phase II comparative purposes (to reflect addition of SINCGARS and AFSATCOM capability for some platforms and deletion of HF as an integrated capability). Recommended development plans were also defined as part of Phase II for the recommended Phase II design.

1.3 STUDY RESULTS, PHASE I

The three Phase I candidate system architectures were compared against the Phase I baseline, with results as shown in Figure 2 and Table 4.

After analysis of both the relative benefits and the relative risks of each approach, candidate system architecture No. 3 was selected by the Government for more detailed design study during Phase II.

The selected architecture No. 3 embodied the most innovative signal processing technology and technique of the three candidate system architectures. The largest contributor to projected system savings was represented by two specific new processor-controlled, time-shared signal processing devices and new signal processing techniques associated with these two new

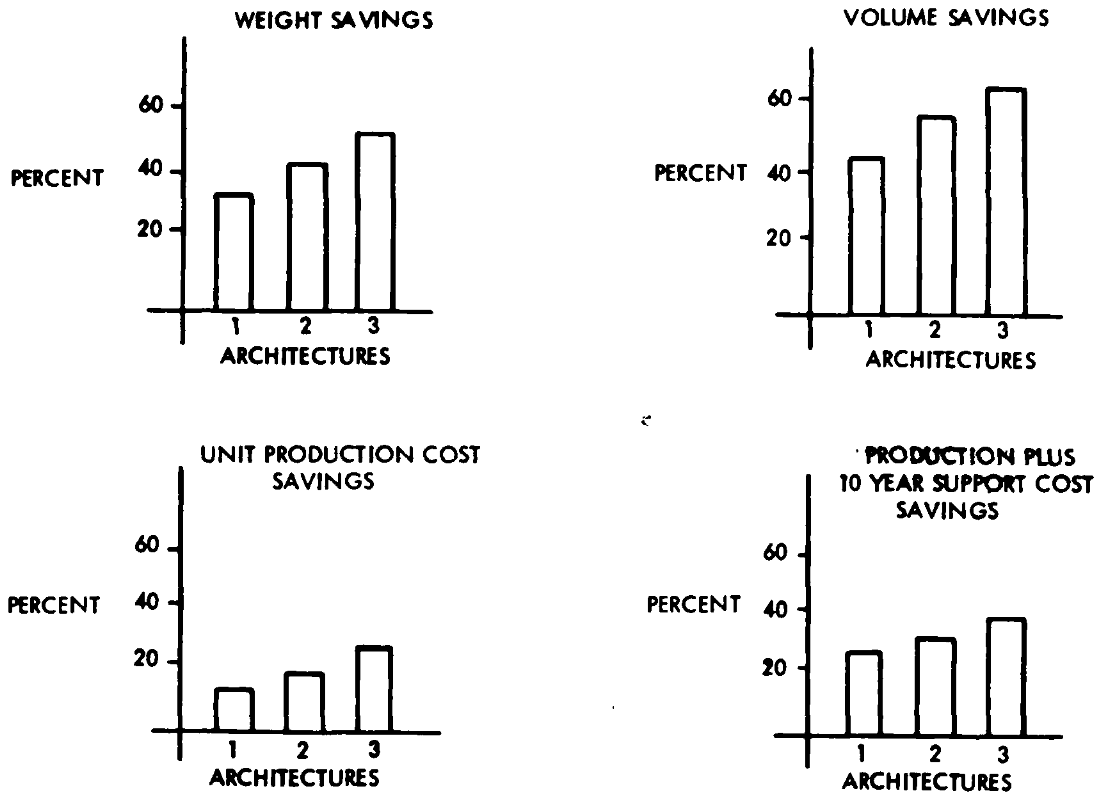


Figure 2. Projected MFBARS benefits for each candidate system architecture, as compared to baseline

TABLE 4. MFBARS PHASE I CANDIDATE ARCHITECTURES COMPARED TO PHASE I BASELINE

	Phase I Baseline	MFBARS No. 1	MFBARS No. 2	MFBARS No. 3
Weight	420#	290#	253#	215#
MFBARS Savings	-	31%	40%	49%
Volume	7.0 cu.ft.	3.9 cu.ft.	3.3 cu.ft.	2.6 cu.ft.
MFBARS Savings	-	44%	53%	63%
Unit Prod Cost (1050 units)	$200K	$176K	$168K	$152K
MFBARS Savings	-	12%	16%	24%
Prod Costs (1050 units) plus Support Costs (10 years)	$302M	$231M	$221M	$203M
MFBARS Savings	-	24%	27%	33%

devices. The new devices were:

- a wideband agile transversal filter (WBATF), and
- a narrowband agile transversal filter (NBATF).

The WBATF enables a unique approach to RF tuning which provides considerable hardware savings over conventional RF tuning techniques. The NBATF enables high speed reconfiguration of flexible signal processing hardware which in turn permits highly efficient hardware time-sharing.

During Phase II, details of these devices and their utilization in the system were refined.

1.4 STUDY RESULTS, PHASE II

The Phase II relative advantages of MFBARS were even greater than projected during Phase I. Figure 3 illustrates the Phase II physical design results, compared to the Phase II baseline. Figures 4, 5 and 6 show packaging details. Table 5 provides a quantitative summary of Phase II design advantages.

Section 2, following, provides design highlights of the Phase II design.

TABLE 5. MFBARS PHASE II COMPARISONS, MFBARS VERSUS BASELINE

	Phase II Baseline	Phase II MFBARS
Weight	455#	161#
MFBARS Savings	-	65%
Volume	6.8 cu.ft.	2.0 cu.ft.
MFBARS Savings	-	71%
Unit Prod Cost* (1050 units)	$327K	$121K
MFBARS Savings	-	63%
Production Costs* (1050 units, plus non-recurring prod costs)	$494M	$161M
MFBARS Savings	-	67%
LCC Costs* (includes development, production, 10 years support)	$575M	$199M
MFBARS Savings	-	65%

*All costs in 1978 $

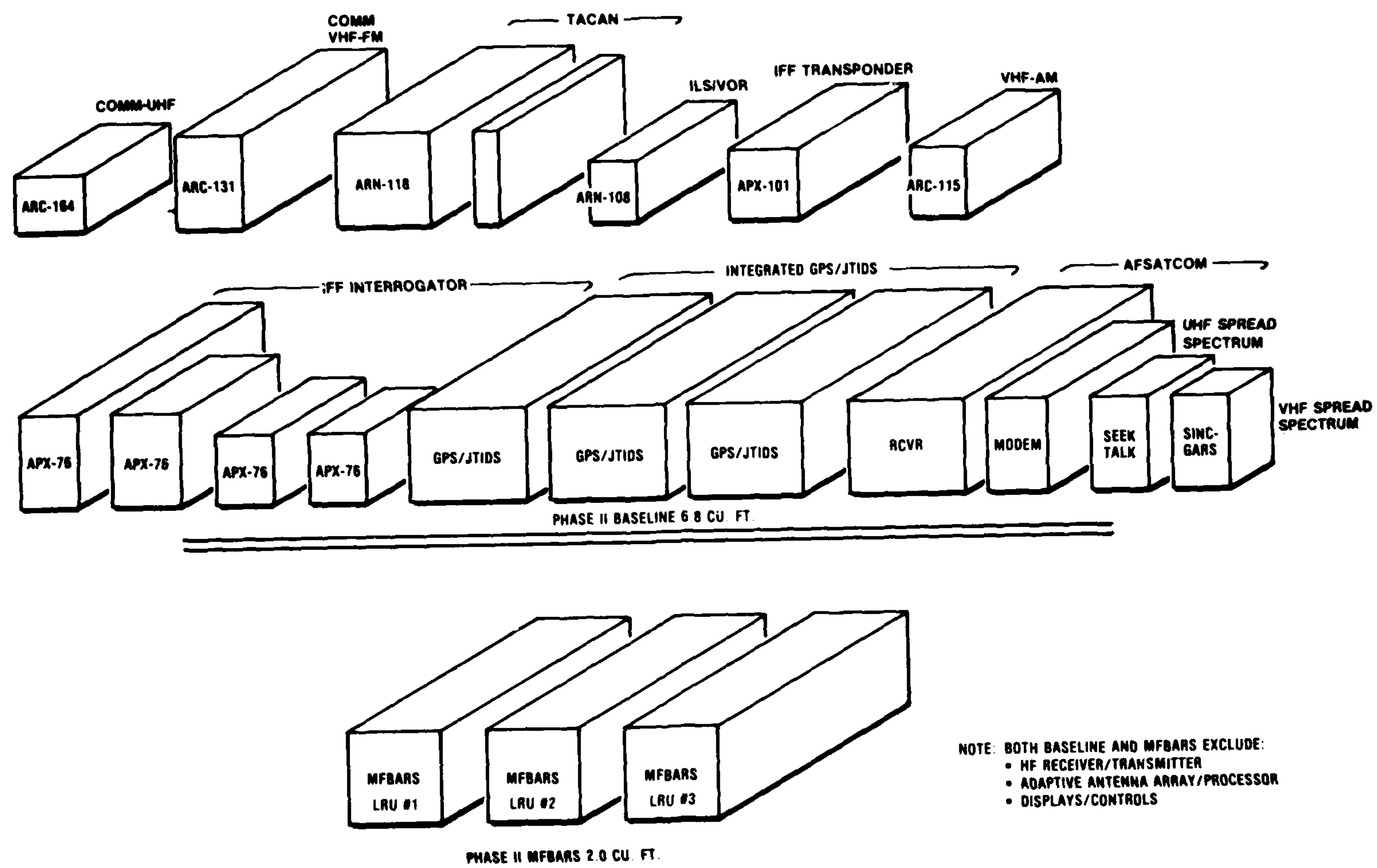


Figure 3. Comparison, MFBARS versus baseline

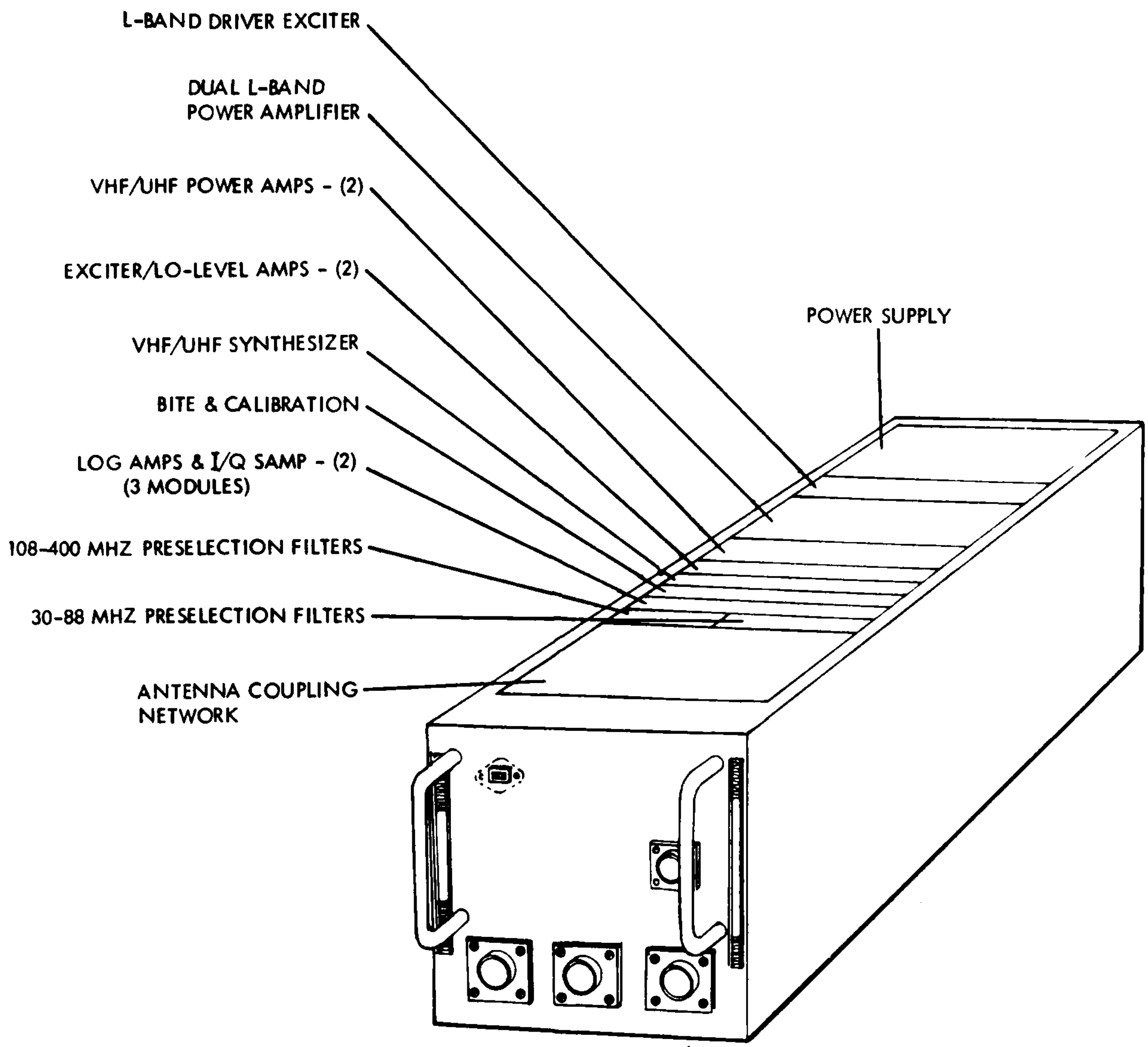


Figure 4. MFBARS Phase II, LRU no. 1

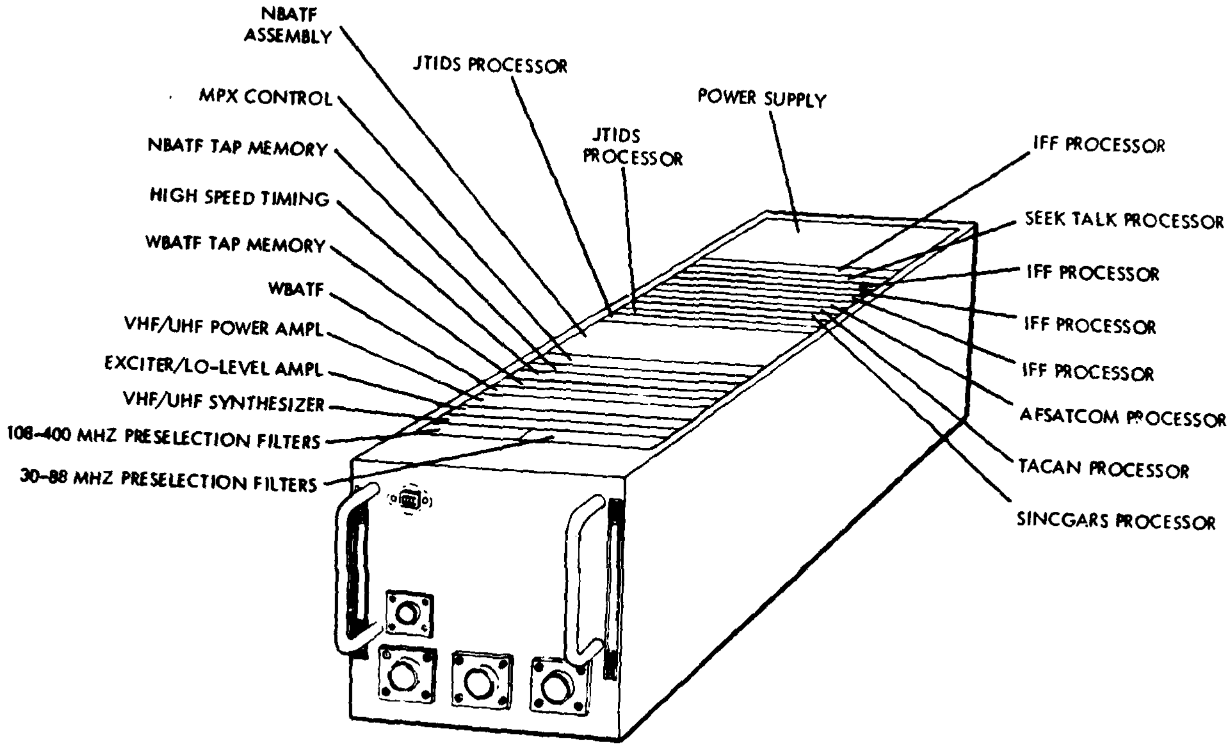


Figure 5. MFBARS Phase II, LRU no. 2

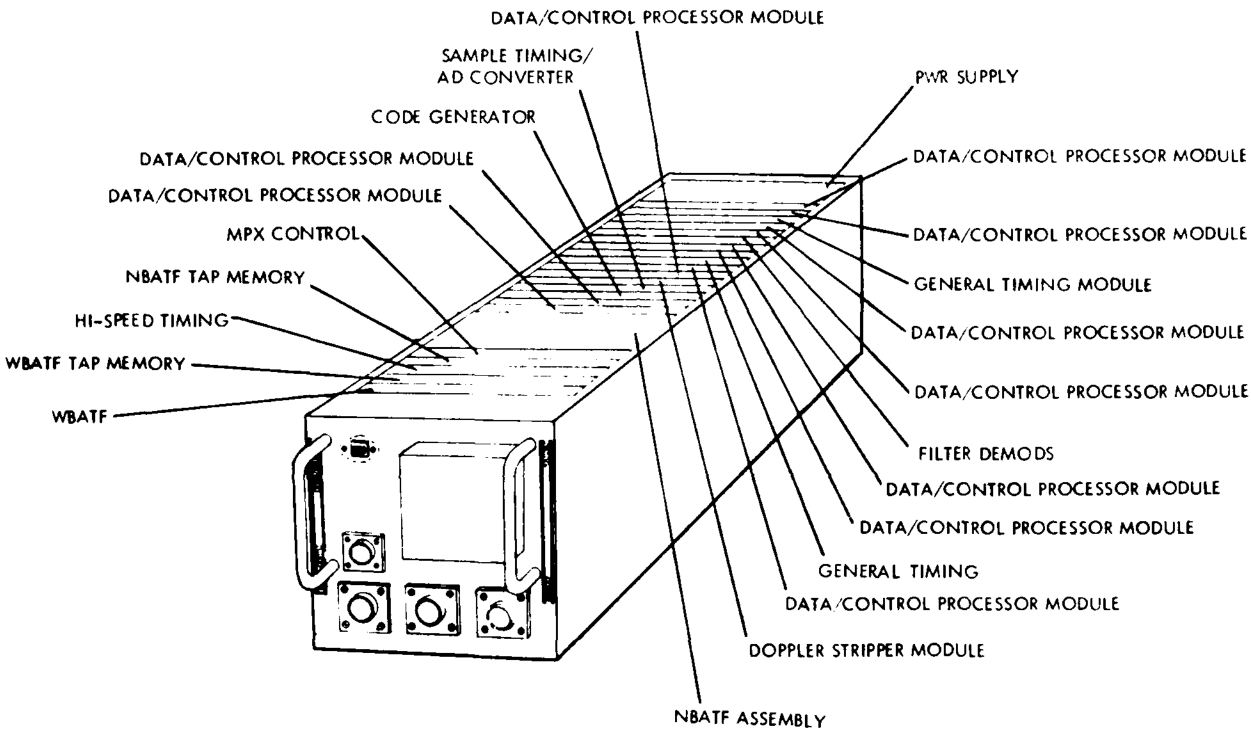


Figure 6. MFBARS Phase II, LRU no. 3

2. HIGHLIGHTS OF PHASE II SYSTEM DESIGN

Figure 7 shows interfaces between MFBARS and other aircraft systems. MFBARS performs all the required radio functions on the aircraft. Non-digital (e.g., audio) information interfaces with the aircraft intercom system. Digital data interfaces with the Digital Avionics Information System (DAIS), which in turn interfaces with the cockpit controls and displays and with other aircraft systems (INS, weapon system and fire control computers, etc.) There is also a direct interface between the Inertial Navigation System (INS) and MFBARS for some signals (e.g. high speed tracking loops).

Figure 8 shows the MFBARS top level block diagram.

The Antenna Subsystem consists of antenna elements, antenna selection switches and antenna coupling circuitry. The antenna elements may be either conventional antenna element or adaptive antenna arrays, depending on the specific type of aircraft. Two adaptive antenna array concepts are still under evaluation. One is a conventional multi-band self-contained adaptive array, with minimum control signal and RF interfaces with the rest of MFBARS. The other is a more highly integrated design concept in which portions of the RF subsystem hardware would be shared with the antenna array processor to achieve a higher degree of total system integration.

The RF Subsystem consists of three transmitters and the MFBARS receiver RF front ends. The RF receiver front ends contain the most innovative devices in the system, a pair of Wide Band Agile Transversal Filters (WBATF's).

The Signal Processor Subsystem contains baseband converters, a Narrow Band Agile Transversal Filter (NBATF) Assembly, a signal switching network, code generators, and special purpose dedicated signal processors.

The Data and Control Processor Subsystem consists of a dynamically reconfigurable multiprocessor array, modularized main memory (in which is stored all system operating programs and the system data base), internal and external input/output devices (I/O's), and an interconnection structure.

The BITE Subsystem is a processor-controlled built-in test subsystem for testing, monitoring and evaluating system health. It contains analog and digital test signal generators and analog sensors and digital logic for determining whether the system is operating within performance limits,

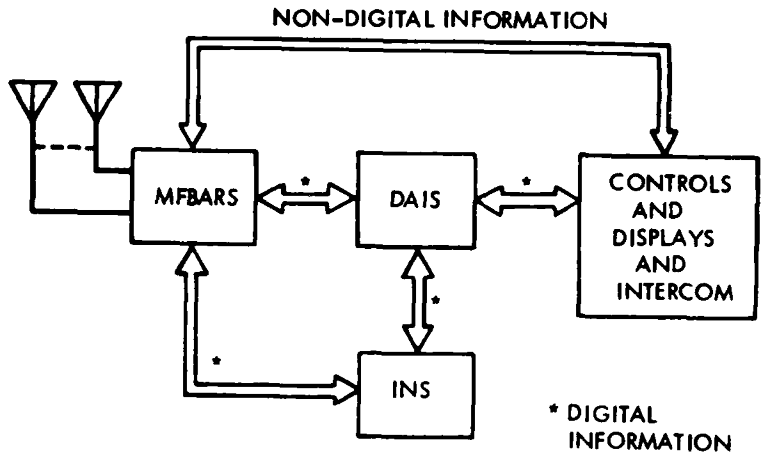


Figure 7. Interface of MFBARS with other aircraft systems

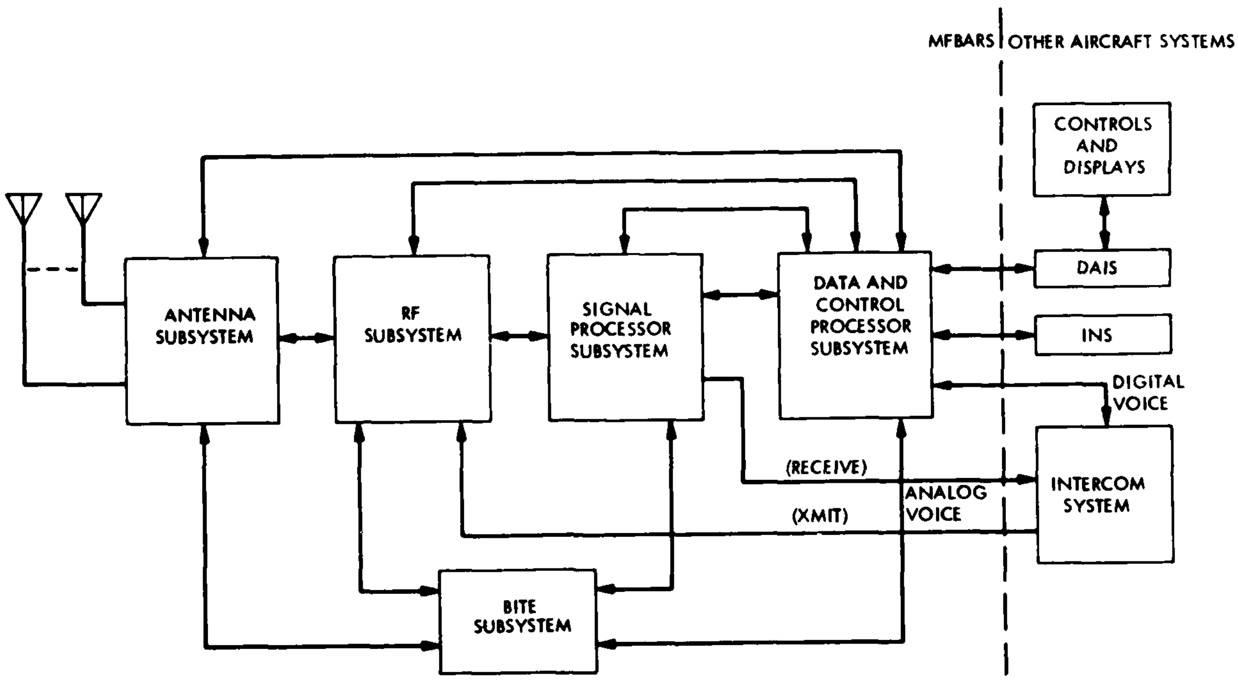


Figure 8. MFBARS top level block diagram

and for fault-isolation in the case of detection of out-of-limit performance. The BITE Subsystem can provide inputs to the Data and Control Subsystem for in-flight system reconfiguration in the event of detected failures.

2.1 ANTENNA SUBSYSTEM

Since MFBARS must operate with both conventional antennas and with adaptive antenna arrays, both options were addressed in the Phase II study. Figure 9 shows the basic antenna requirements. Figure 10 shows nominal aircraft location of conventional antennas. Three of the signals (GPS, JTIDS, SEEK TALK) are spread spectrum signals, for which adaptive antenna arrays are being developed (under other Government sponsored development programs). For platforms using arrays for one or all of these signals, the conventional antennas would have to be supplemented by one or more arrays.

Figure 11 shows separate, non-integrated, arrays for each spread spectrum signal. This represents the lowest technical risk approach for use of arrays, but imposes severe problems in terms of aircraft integration and does not provide for any cost savings through sharing of common antenna element and/or antenna array processor hardware. A more innovative array approach would be a single integrated array. This approach would reduce aircraft integration problems and would allow sharing of common antenna element hardware, but would represent higher technical risks and development costs. This approach is shown in Figure 12. Two such arrays would be required per platform, one on the top and one on the bottom.

Another level of integration is also possible wherein the adaptive array processor would be integrated with the RF front end processor to achieve processor hardware sharing economies. Frequency up- and down-translation would be required for this approach, as illustrated in Figure 13. In addition, the WBATF's used in the RF Subsystem would be moved to the Antenna Subsystem, as shown in Figure 14, for the purpose of integrating antenna array processor and RF processor hardware. This design approach is still under evaluation. It offers the highest level of savings through integration, but is a substantial departure from conventional interfaces between the Antenna Subsystem and the RF Subsystem.

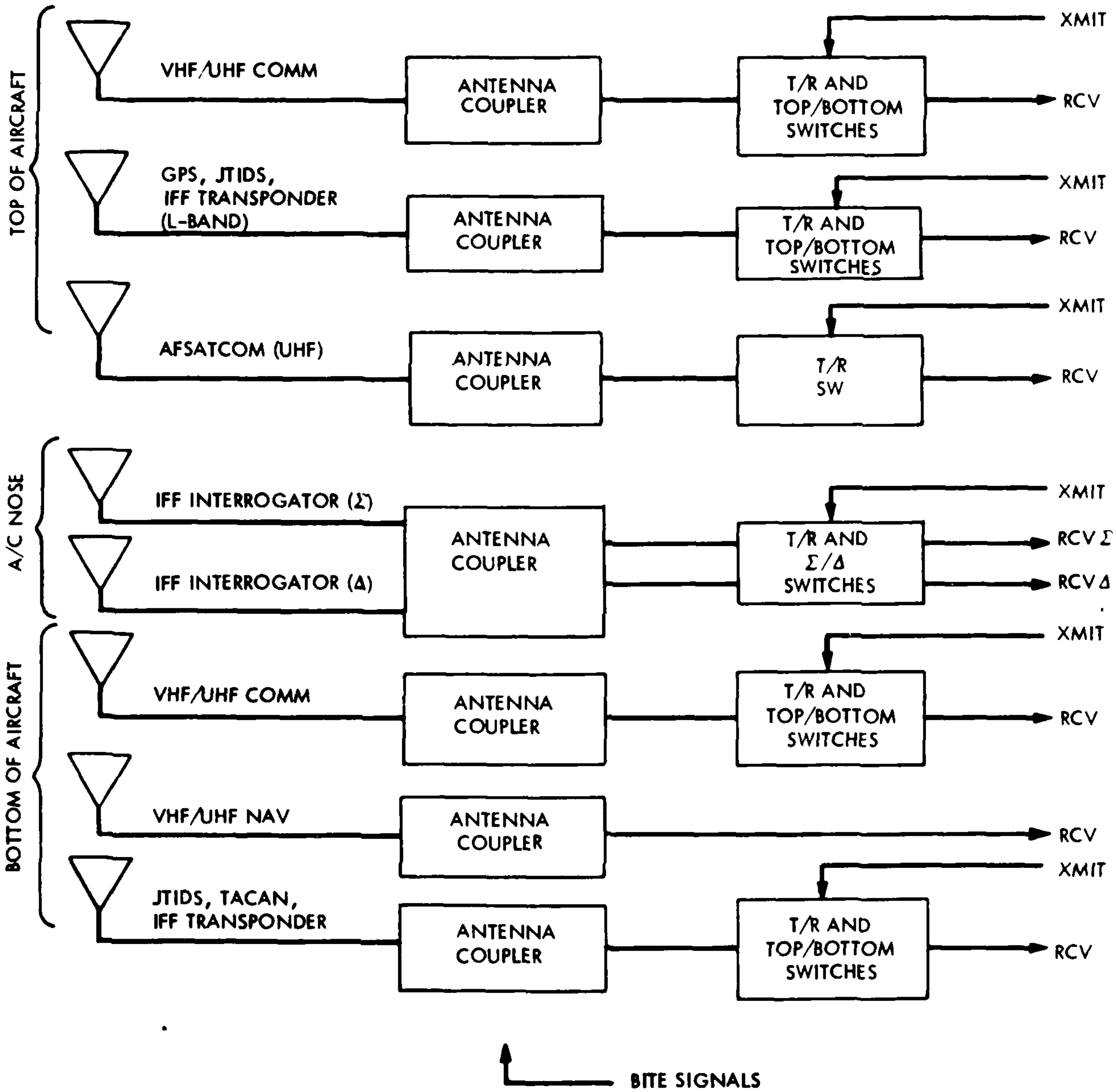


Figure 9. Antenna Subsystem

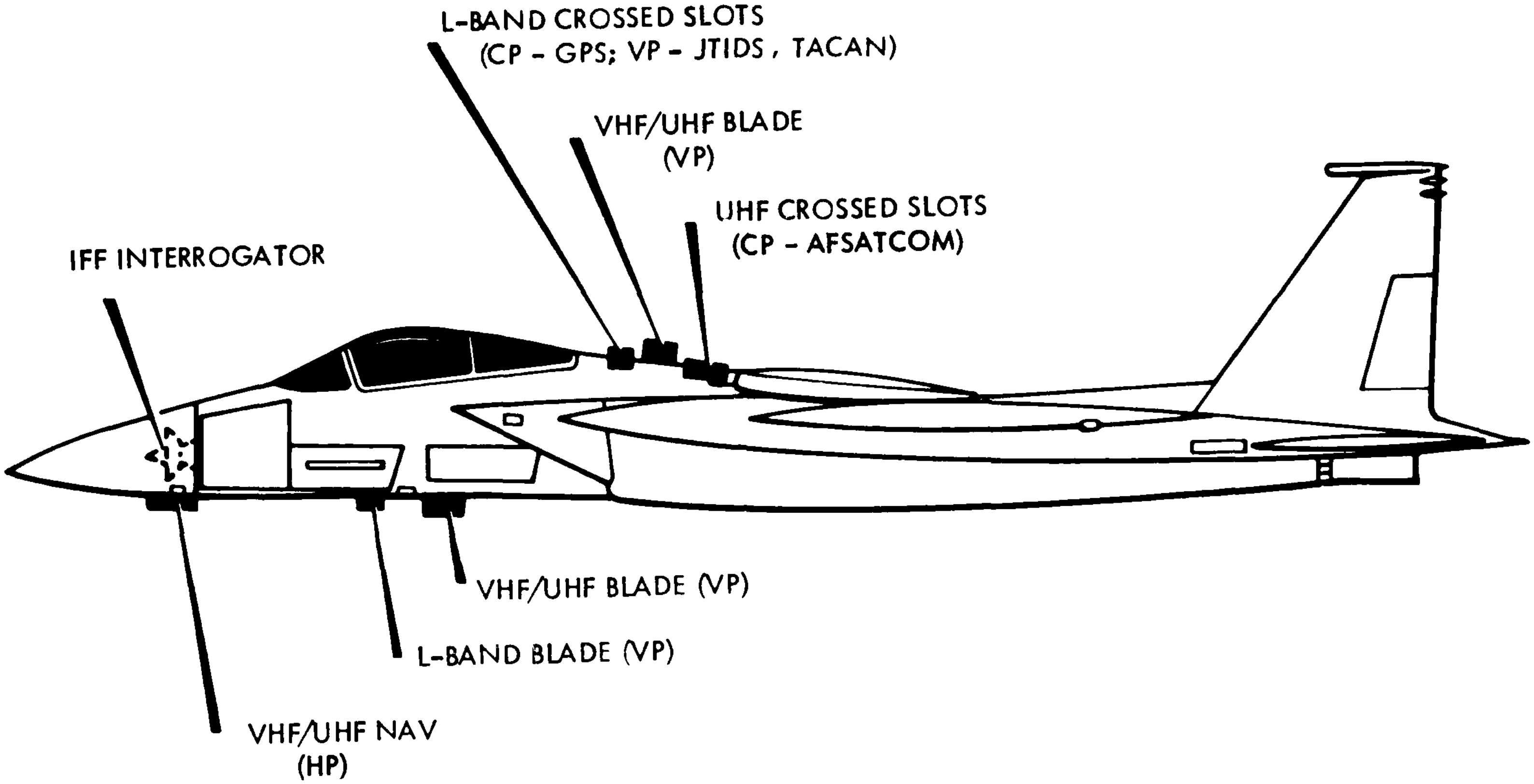


Figure 10. Nominal antenna locations, conventional antennas

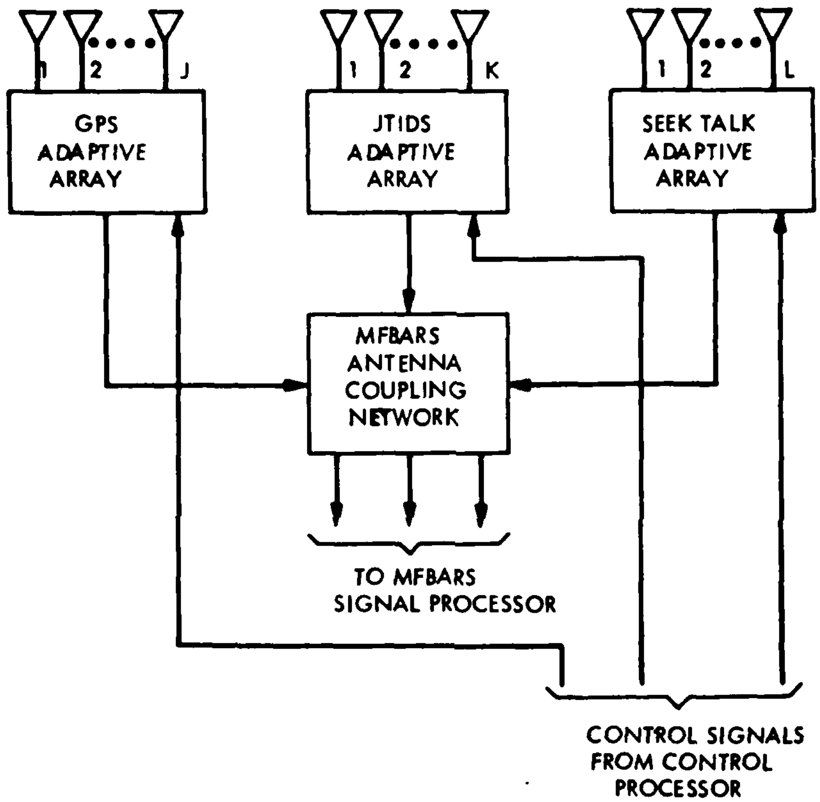


Figure 11. A non-integrated approach to adaptive arrays

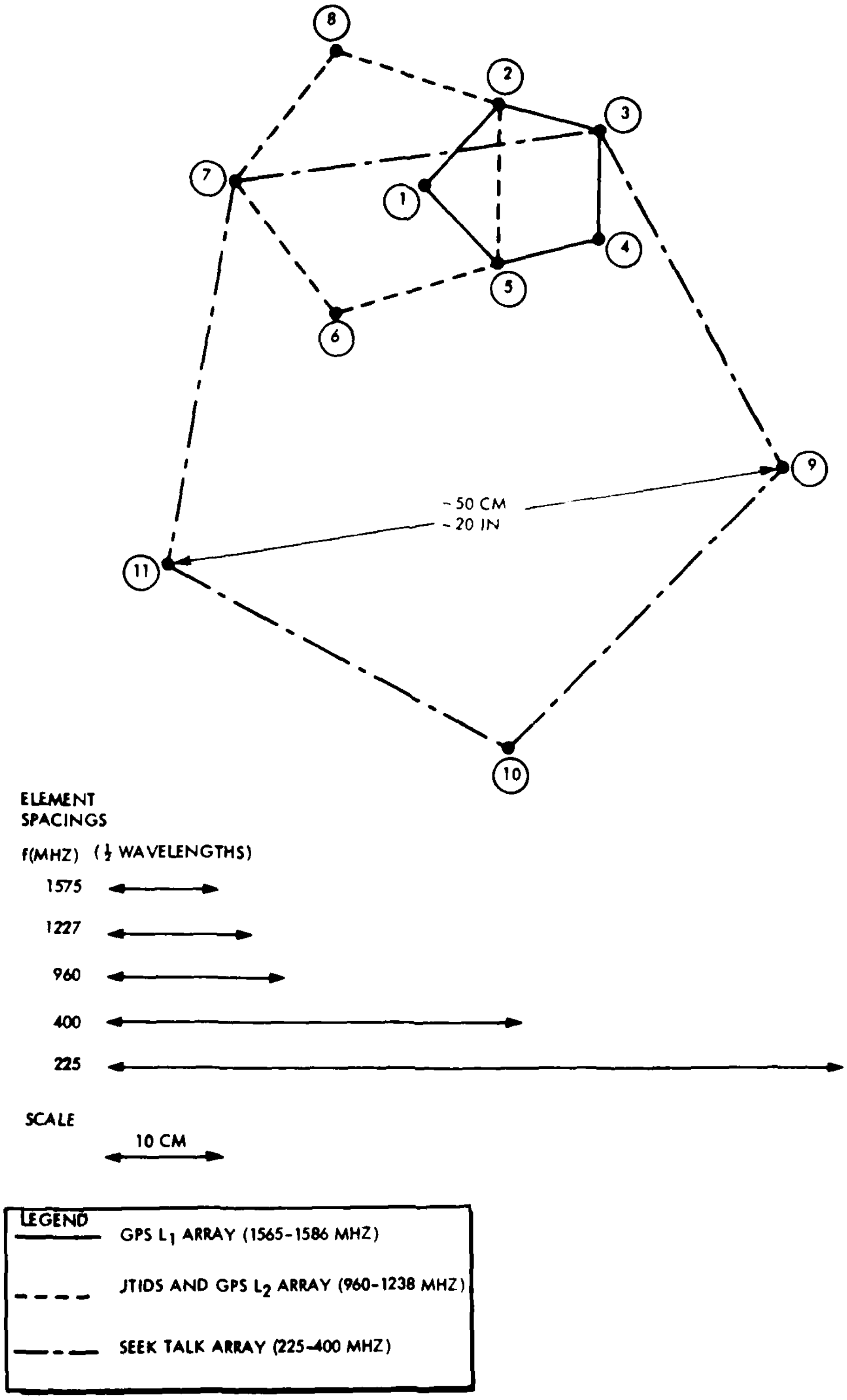


Figure 12. Eleven element array concepts

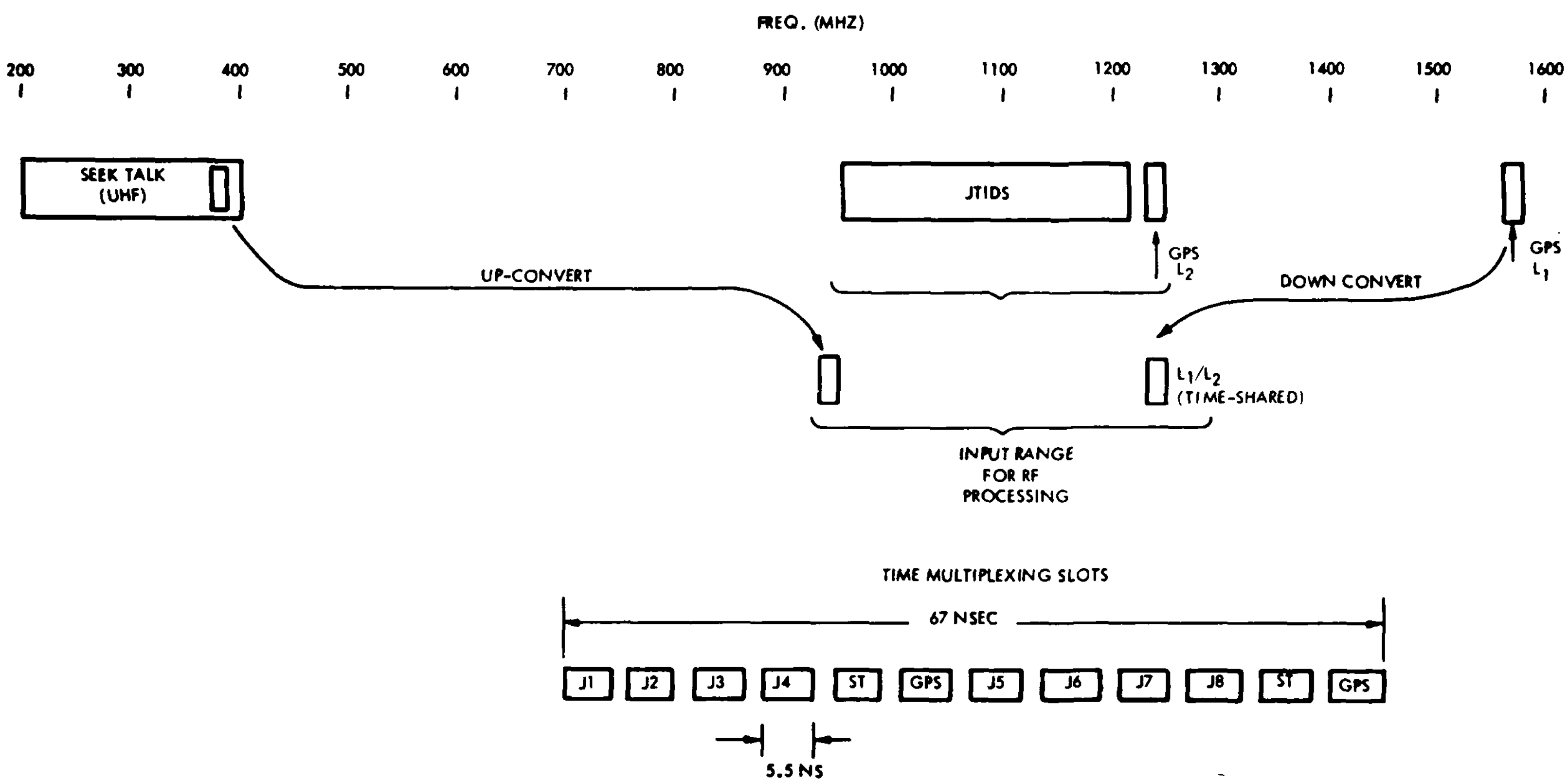


Figure 13. Time-sharing and up/down conversion for integrated processing

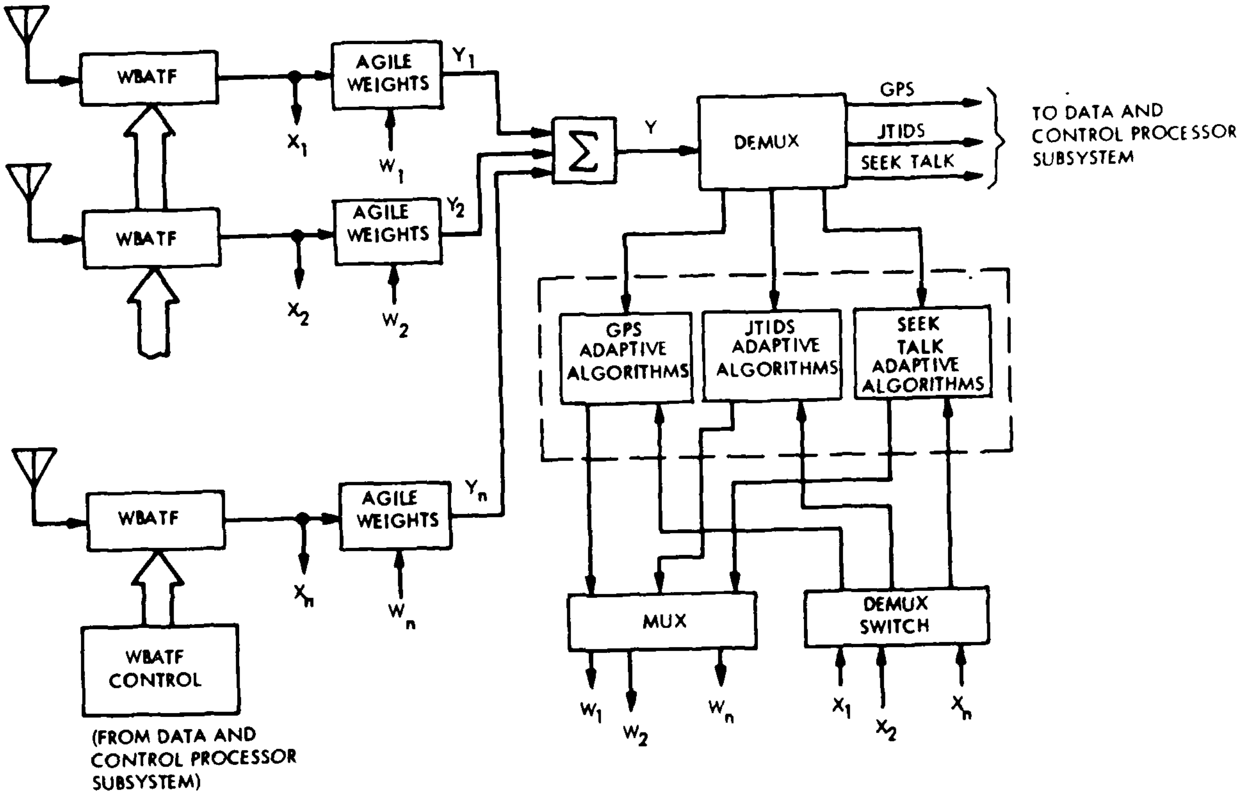


Figure 14. Integrated adaptive antenna array processor/ spread spectrum RF processor

2.2 RF SUBSYSTEM

The RF Subsystem consists of RF receiver front-end hardware and three transmitters. Figure 15 shows a top level block diagram of the RF Subsystem.*

The RF Subsystem contains the most innovative device technology utilized by MFBARS, a pair of wideband agile transversal filters (WBATF's). The WBATF's allow the system to use direct frequency tuning for variable tuned signals, rather than superheterodyne techniques. This is one of the major contributions to MFBARS hardware simplification, which in turn provides significant MFBARS system size and cost savings.

Note from Figure 15 that the GPS L_1 and L_2 signals and IFF signals are shown as bypassing the WBATF's. This is because they are fixed frequency signals, for which conventional fixed frequency bandpass filters are adequate for signal selection. (The WBATF provides greatest efficiencies for variable tuned signals, rather than fixed tuned signals.) However, alternate configurations are still under consideration. It may turn out better for overall tradeoff reasons to also have the WBATF's select the GPS and IFF fixed frequency signals, as well as the variable-tuned signals. Tradeoffs in subsequent phases of the program will determine the best final configuration.

2.2.1 Wideband Agile Transversal Filters (WBATF's)

The heart of the selected MFBARS architecture is an advanced technology device called a wideband agile transversal filter (WBATF). A WBATF is a special form of a generic device called a transversal filter, which is a device containing:

- a lossless delay line through which an input signal propagates
- a large number of equally spaced lossless taps which sense signal energy as the input signal traverses the taps

*Note from the previous section that one of the adaptive antenna array concepts being considered would change the conventional boundary lines between the Antenna Subsystem and the RF Subsystem. If this approach were to be implemented, there would be two different RF Subsystem configurations for MFBARS: (1) a highly integrated configuration for those aircraft having adaptive antenna arrays; and (2) a conventional configuration for those aircraft not having adaptive antenna arrays.

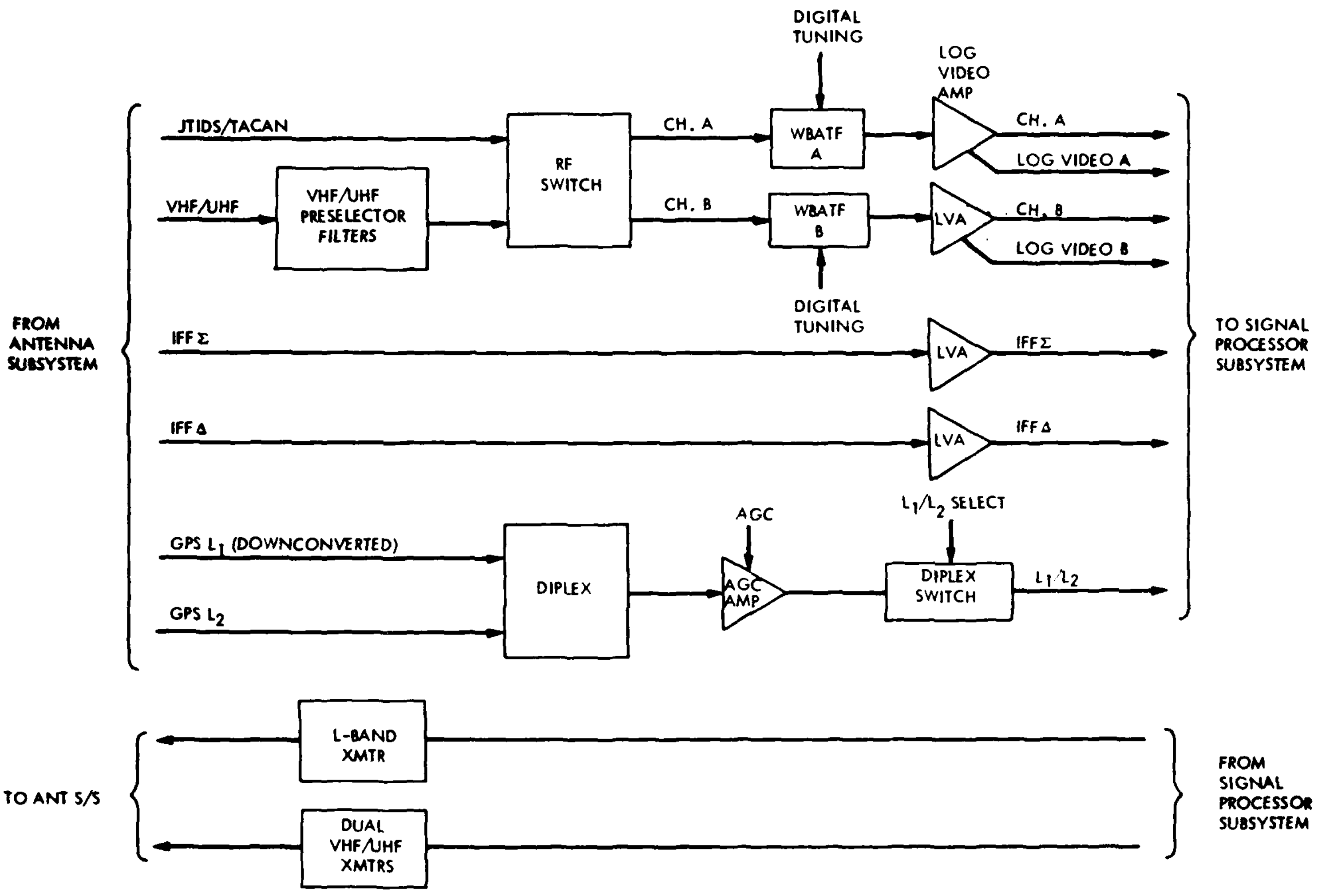


Figure 15. RF Subsystem

- tap weights, one for each tap
- a summing bus output, which sums the weighted energy detected by the taps.

If the incoming RF contains a signal whose shape matches the predetermined reference shape stored in one of the tap weight sets, then the summing bus output will peak during the sampling interval. If there is no match, the weighted tap outputs will tend to randomly cancel out and the summing bus will not peak. Amplitude measurement of the summing bus outputs can provide successive samples of detected signals of interest. These successive samples are at rates greater than the Nyquist rate of the signals of interest, so that the outputs will be (multiplexed) samples of the modulated waveforms of the signals of interest. The multiplexed sampled waveforms can then be demultiplexed in subsequent MFBARS circuitry so that each signal of interest can be processed separately.

The major differences between the generic transversal filter and the WBATF are: an extraordinarily wide input bandwidth (400 MHz); high speed sampling of the input signal (870 MHz); a large number of taps (500); and the ability to change the tap weights rapidly (6 ns), under software control, as the sampled signal propagates through the device. The usual transversal filter either has fixed tap weights which cannot be changed at all or tap weights which can be changed only slowly relative to the propagation time of the input signal through the delay line. By contrast, the WBATF weighting circuits can be changed at a high rate relative to input signal transit time through the delay line. With this capability, the tap weight reference characteristics can be changed at several times the Nyquist sampling rate (for all signals of interest) as they propagate through the delay line. This allows high speed switching between several different tap weight references during signal transit through the delay line. Thus, several different signals of interest can be sampled, on a time multiplexed basis, during propagation through a single WBATF. Most importantly, there is no signal to noise degradation in these multiplexed samples, because of the Nyquist sampling and because the tap process is lossless. These features provide the ability for a WBATF-equipped MFBARS to offer considerable savings in hardware for multiple signal tuning, compared to conventional RF tuning approaches.

Figure 16 shows a general block diagram of the WBATF. As an input signal travels through the delay line, the summing bus output provides successive instantaneous summations of the input signal, as shaped by the tap weights, which are set by the tap weight register. The tap weights can be

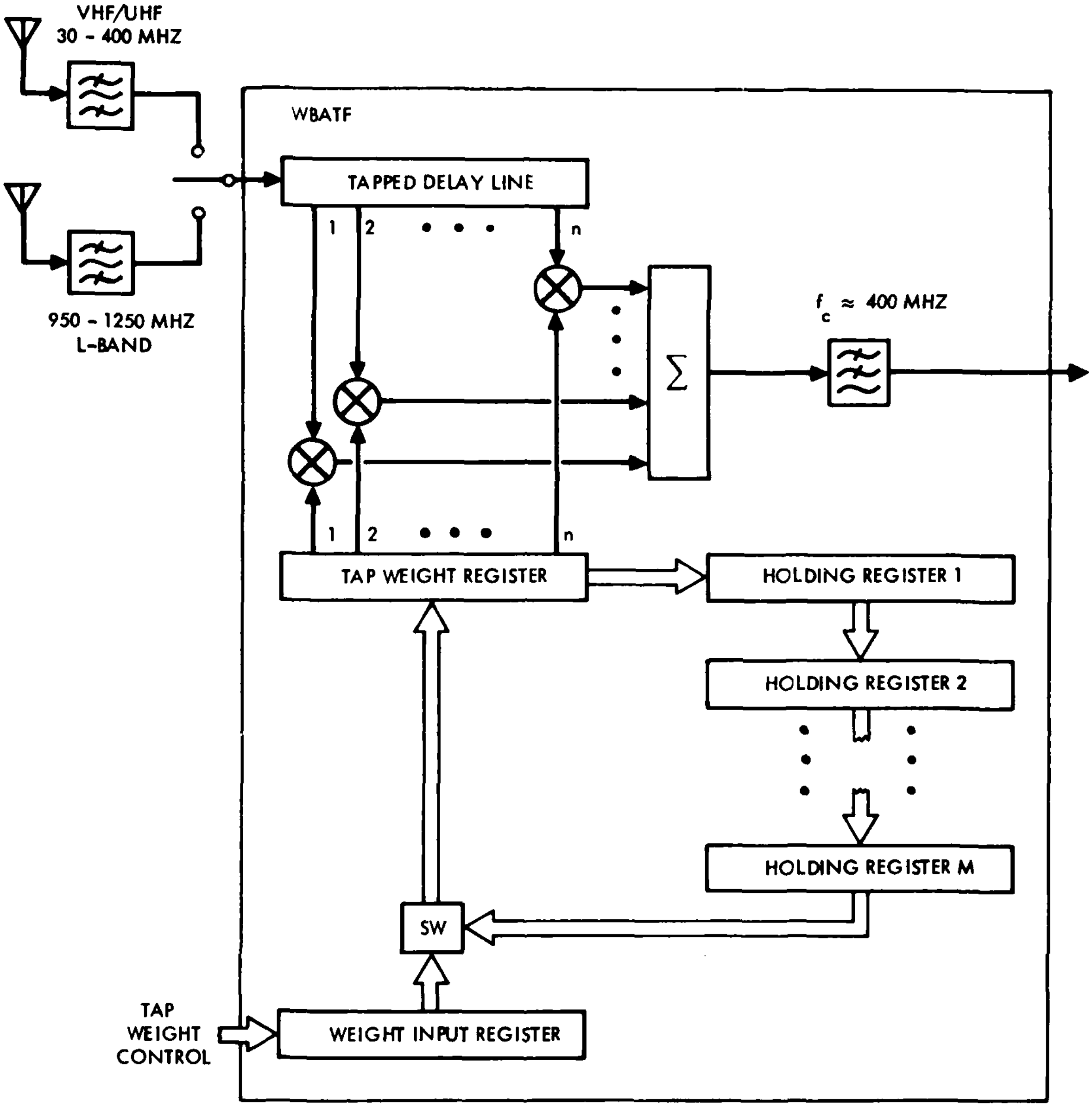


Figure 16. WBATF block diagram

changed by input control signals to provide different sets of tap weights for several selected signals of interest. As shown in Figure 16, multiple sets of tap weights can be pre-stored in holding registers within the WBATF. These several sets of tap weights are then advanced one set at a time to the tap weight register, where they reset the tap weights for one sampling interval. Then a different set of tap weights is advanced to set the weights for the next sampling interval, and so on. Any pre-stored set can be replaced at any time by control inputs, so that any new signal reference can replace any prior signal of interest reference at any time.

The WBATF performs the following functions for the selected MFBARS architecture.

- It provides a capability for high speed (multiplexed) switching (tuning) between several different frequencies of interest.

- It is fully programmable in terms of center frequency and bandshape, making it useful for processing various signal formats in a multi-function environment.

As shown in Figure 15, the selected MFBARS architecture contains two identical WBATF's, one for L-band signals and one for VHF/UHF signals. Each has an RF input bandwidth of aproximately 400 MHz. Either WBATF can be switched to the other band, or either can handle both bands, on a multiplexed basis. This flexibility provides fail soft system degradation in the event of failure.

2.3 SIGNAL PROCESSOR SUBSYSTEM

The Signal Processor Subsystem consists of two baseband converters, a signal switching network, a narrowband agile transversal filter (NBATF) Assembly, code generators, and special purpose dedicated signal processors. Figure 17 shows a top level block diagram of the Signal Processor Subsystem.

The baseband converters are frequency translation devices, similar in function to a down-conversion mixer, which convert signals to zero-IF for baseband processing. They provide final frequency translation of signals not converted to zero-IF and/or baseband in the WBATF's. (Only those signals whose carrier frequencies are exact multiples of the WBATF sampling rate are translated directly to baseband in the WBATF's.) Figure 18 shows a baseband converter block diagram. Technology required for this device is similar to that developed for the WBATF, but a new circuit design is required specifically for MFBARS application.

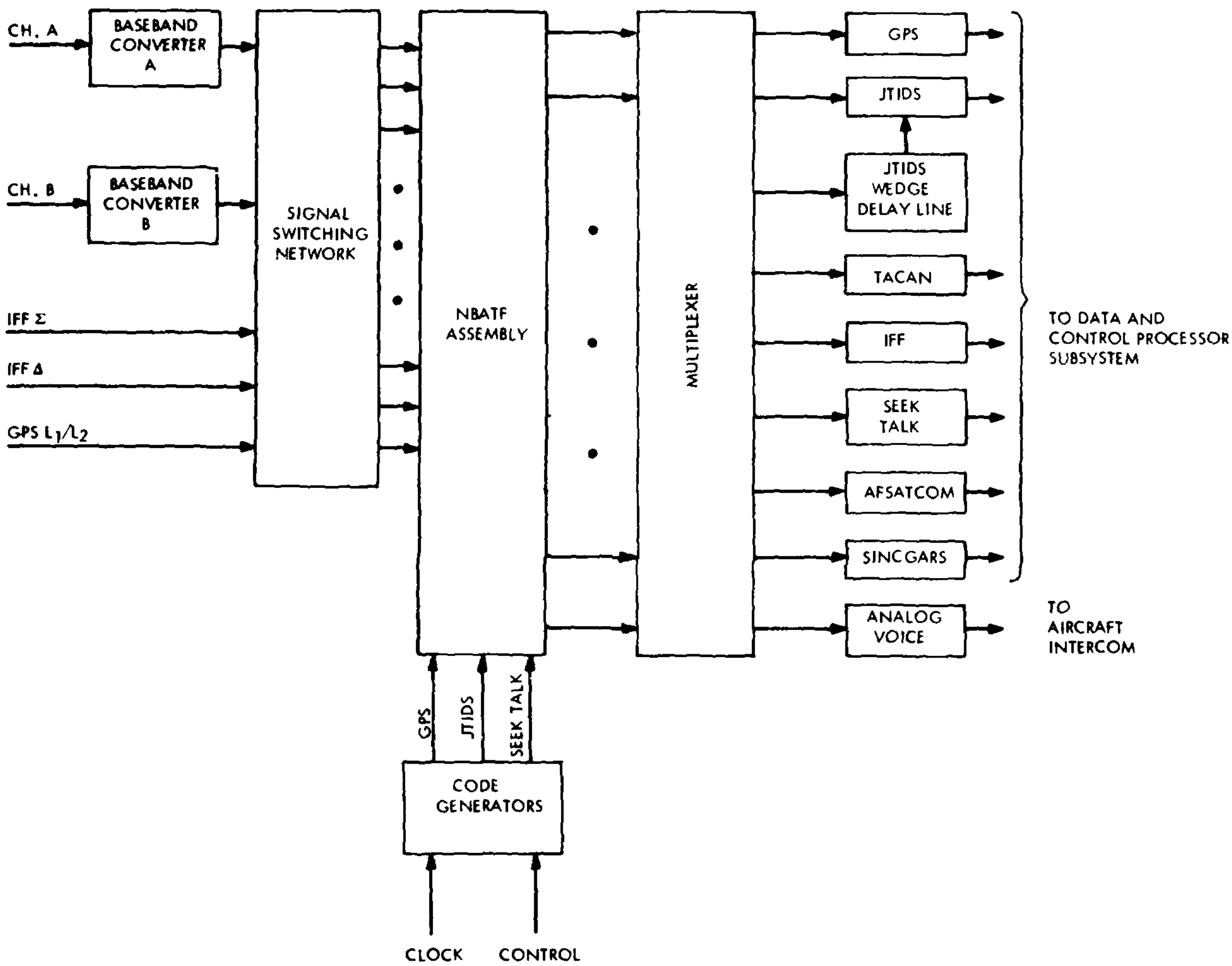


Figure 17. Signal Processor Subsystem

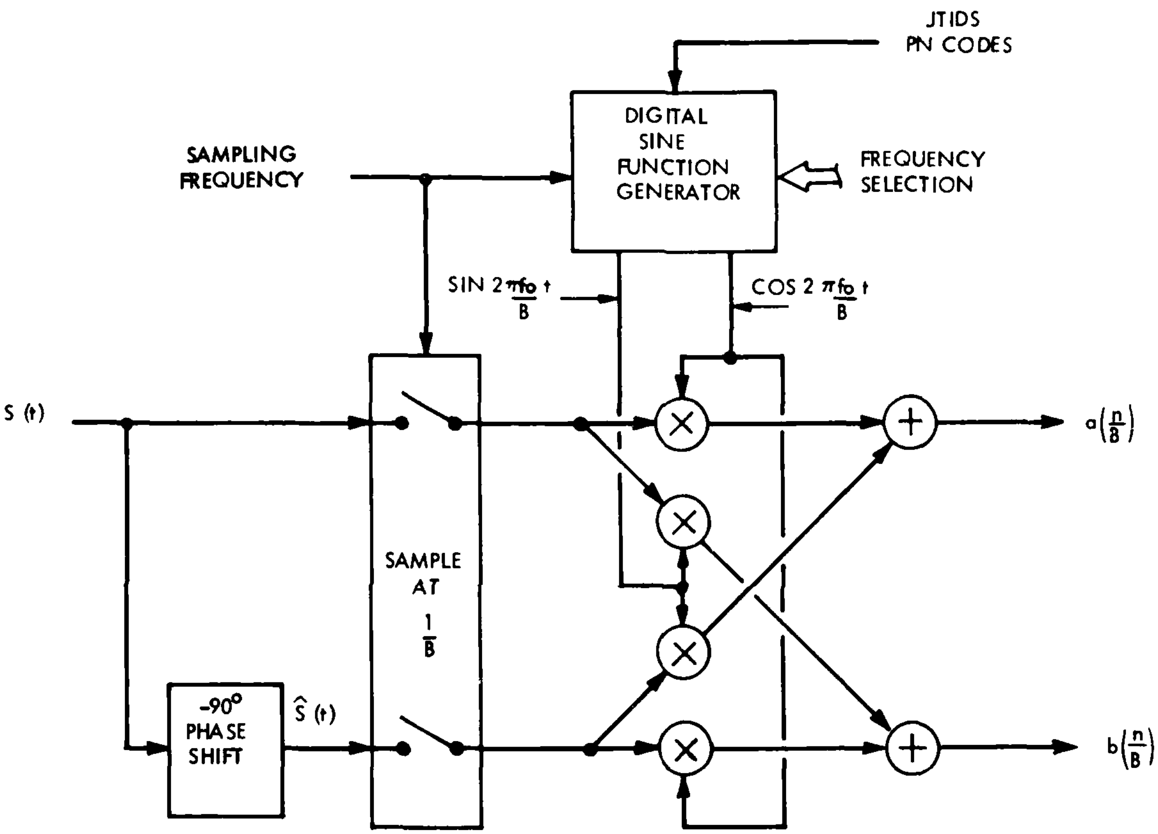


Figure 18. Baseband converter

The signal switching network is a signal routing device which, in conjunction with other circuitry, provides the high degree of flexibility required in a multi-function radio system. This flexibility is achieved through the ability to dynamically reconfigure the system resources to meet the requirements of a particular mission profile, to minimize single point failure modes, and to generally improve significantly the probability of mission success.

Figure 19 is a simplified block diagram of the signal switching network.

The NBATF Assembly provides for flexible baseband signal processing. Further bandlimiting is required following the baseband converter and the signal switching network. Bandwidths of from 5 to 15 MHz must be reduced to bandwidths of as little as 25 kHz, commensurate with IF bandwidths in conventional radios, prior to information band processing. In addition, the spread spectrum signals (GPS, JTIDS, SEEK TALK) must be "despread" by correlation with PN spread spectrum references. Both processes (bandlimiting and PN despreading) can be accomplished with a common device, a narrowband agile transversal filter (NBATF). The NBATF is similar to the wideband agile transversal filter (WBATF) described previously, but operates at slower clock speeds (approximately 30 MHz maximum versus 870 MHz for the WBATF). The NBATF utilizes variable input clocking rates and flexible input/output interconnections.

Figure 20 shows a block diagram of an NBATF. It is a CCD-type device, with 195 taps and an adjustable input clocking rate. Tap weights can be changed, under processor control, to provide variable bandpass shaping and/or variable PN code references for PN correlation. Each NBATF has a capability for storing up to four sets of tap weights for cyclic utilization. New tap weight inputs are entered under processor control. NBATF's are used in sets, with inputs and outputs of each set interconnected as required for optional cascading, optional parallel in-phase and quadrature-phase processing, and/or optional squaring and summing of outputs, according to specific processing requirements for each different type of MFBARS signal being processed (as explained below). Since a good many of the MFBARS signals require four NBATF's or multiples thereof, it is convenient to configure the NBATF's in standard building block sets of four. Figure 21 shows a standard NBATF building block, including the standard flexible interconnections. It is projected that, by the production phase of the program, it may be cost effective to put each set of four NBATF's and their associated support circuits and flexible interconnections on a single monolithic chip.

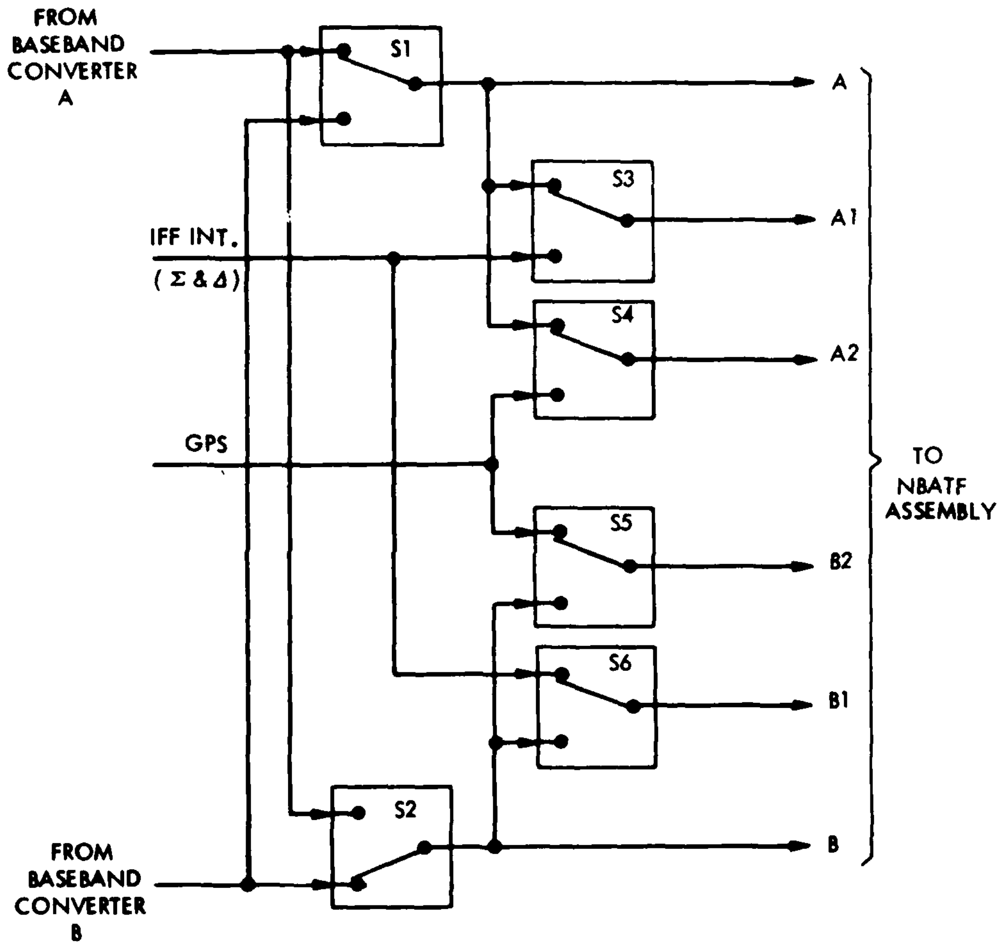


Figure 19. Signal switching network

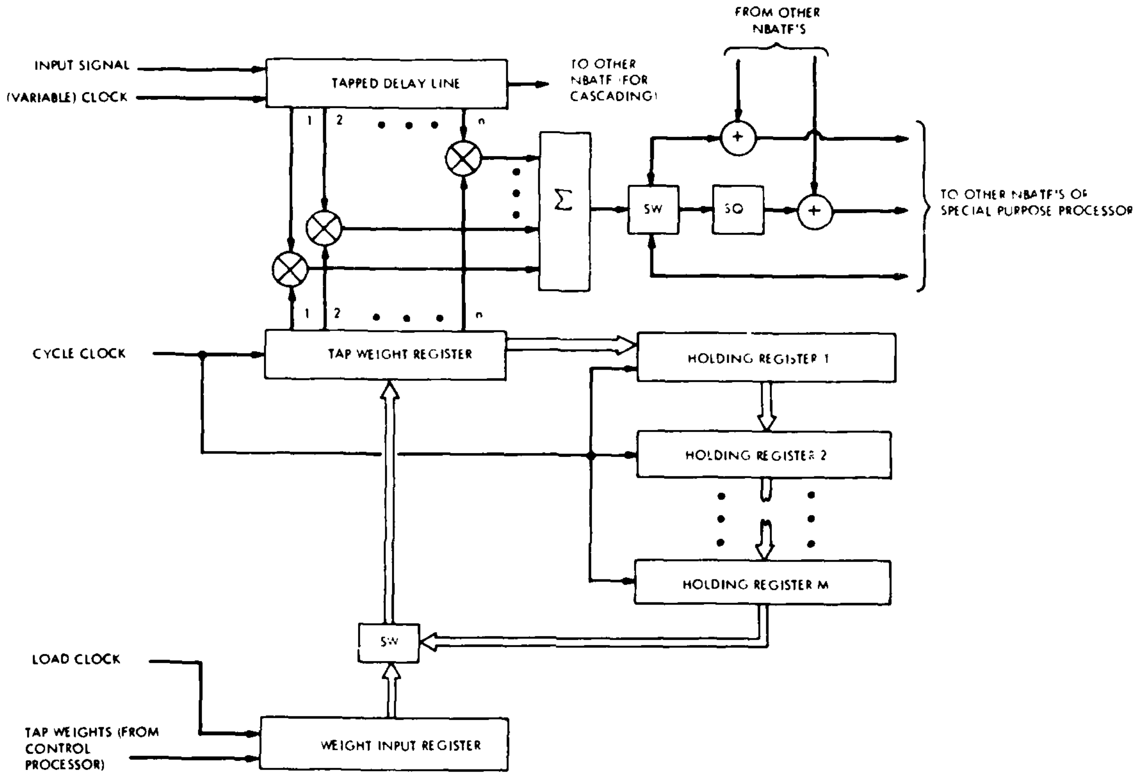


Figure 20. NBATF block diagram

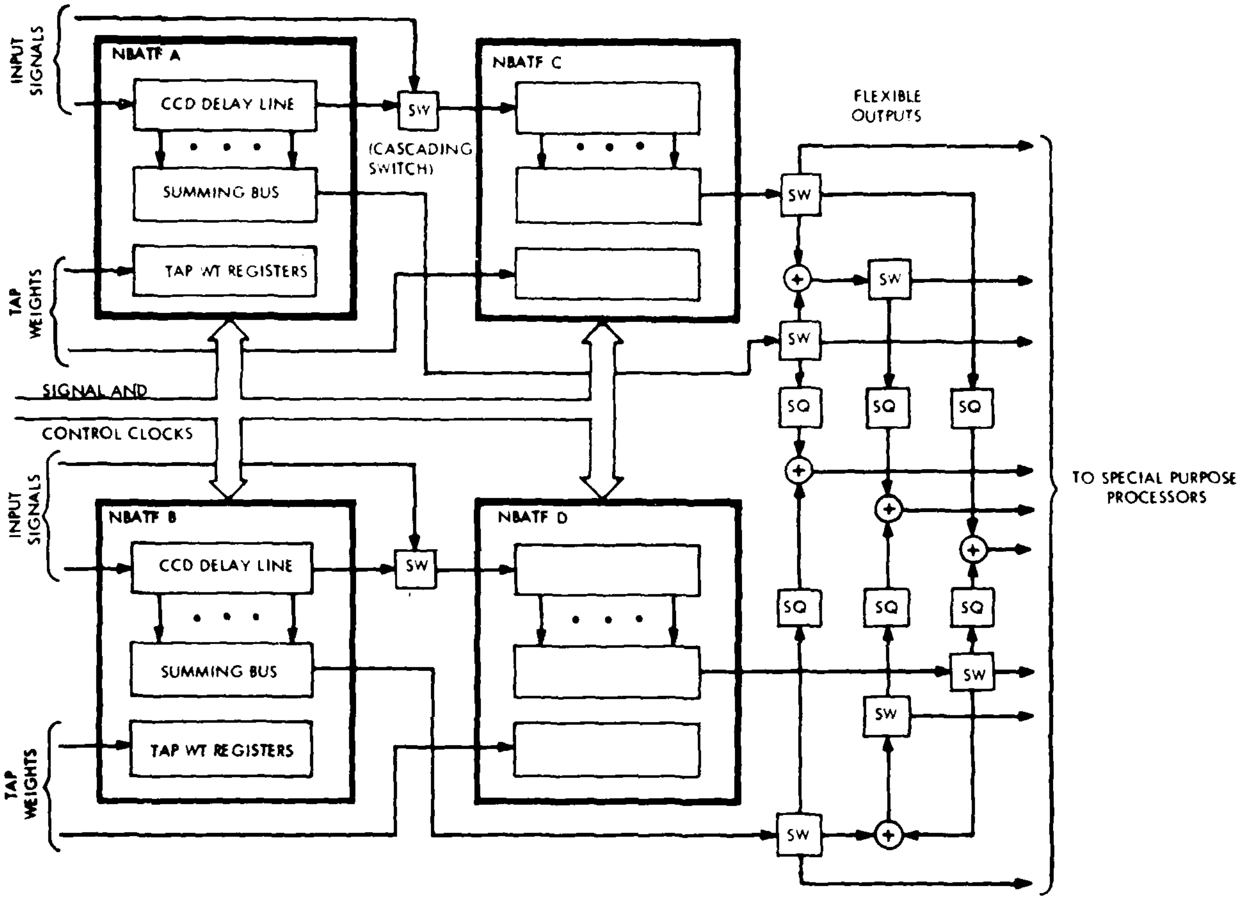


Figure 21. Standard NBATF building block

All of the NBATF building blocks taken together constitute what is referred to as the NBATF Assembly, as shown in Figure 22. Although there is only one NBATF Assembly for MFBARS, each NBATF building block is separately accessible, for system reliability purposes. Since each NBATF building block in the assembly is identical, any signal may be processed by any NBATF building block(s) as assigned under processor control. This provides for fail-soft system operation in the event of failure.

The total number of NBATF building blocks in the NBATF Assembly has not yet been determined, primarily because applicable SEEK TALK design information is not available and because the Government has not yet made a final choice on which form of JTIDS will be utilized, both of which may affect requirements. It is estimated that approximtely 20 NBATF building blocks (with four NBATF's per building block) represent a reasonable upper limit. However, since it is possible to time share NBATF's for some signals, the final number is expected to be less than 20. Table 6 summarizes the NBATF requirements for the system. Figures 23 through 29 then show specific NBATF building block configurations for each type of MFBARS CNI signal.

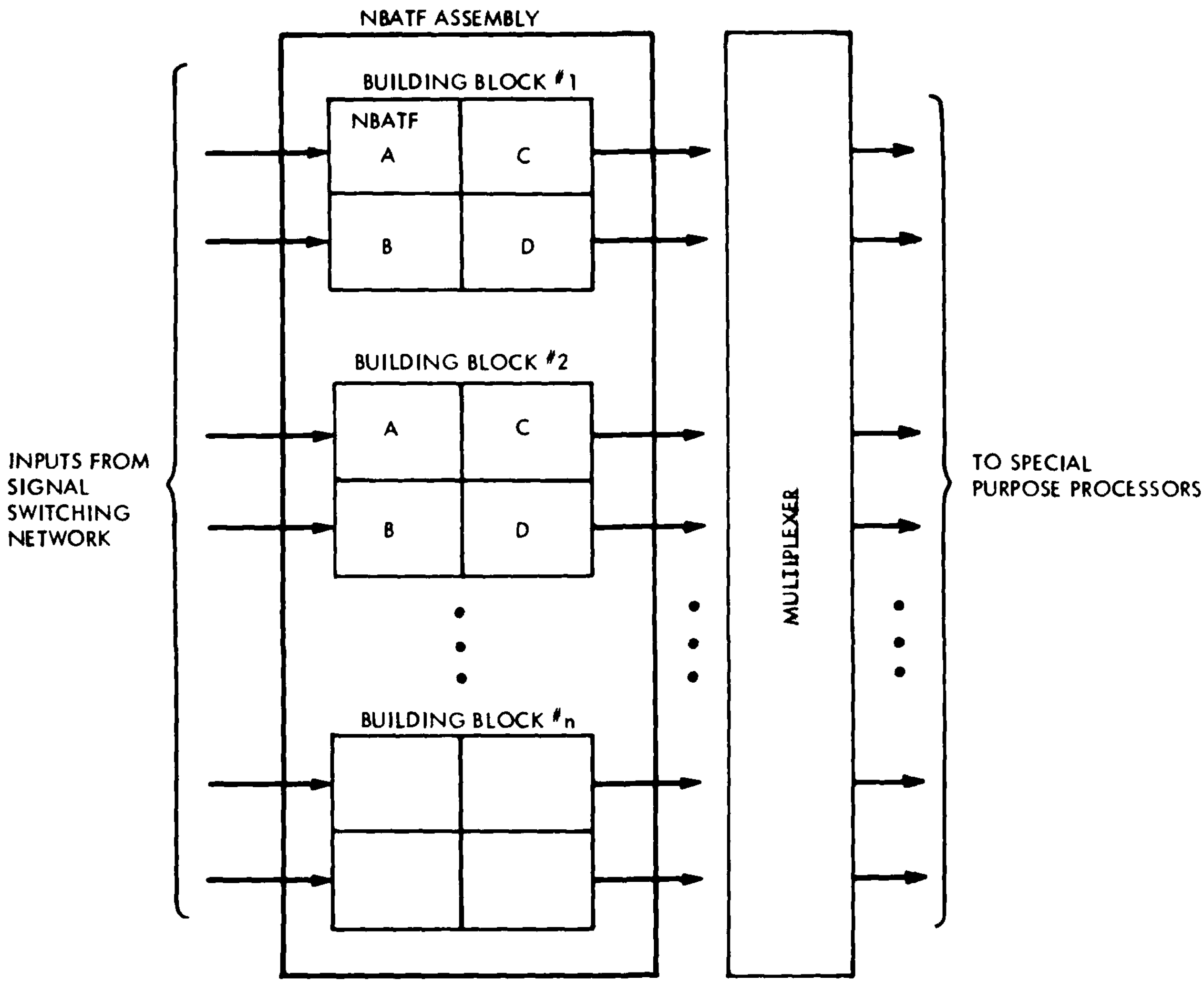


Figure 22. NBATF Assembly

Table 6. NBATF BUILDING BLOCK REQUIREMENTS

	NATF Building Blocks	NBATF's Utilized	Comments
JTIDS, ATDMA/TDMA, Sync	4	16	12 NBATF's available for other signals except during sync.
JTIDS, ATDMA/TDMA, Data	1	4	
JTIDS, DTDMA, Sync and Data	2	8	All 8 required for both data and sync
JTIDS Subtotal	2-4	8-16	
GPS	1	4	
TACAN	1	3	1 NBATF available for other signals
IFF	1	3	1 NBATF available for other signals
SEEK TALK	4	16	(estimated)
VHF/UHF Comm	3	12	
VHF/UHF Nav	1	4	4 time-shared signals
Subtotal	13-15	50-58	
AFSATCOM	1	4	some platforms only
SINCGARS	1	4	some platforms only
	15-17	58-66	
VHF FM homing	(1)	(4)	backup nav
VHF AM ADF	(1)	(4)	backup nav
UHF AM ADF	(1)	(4)	backup nav
	(15-17)	(58-66)	(backup nav not an additive NBATF requirement)

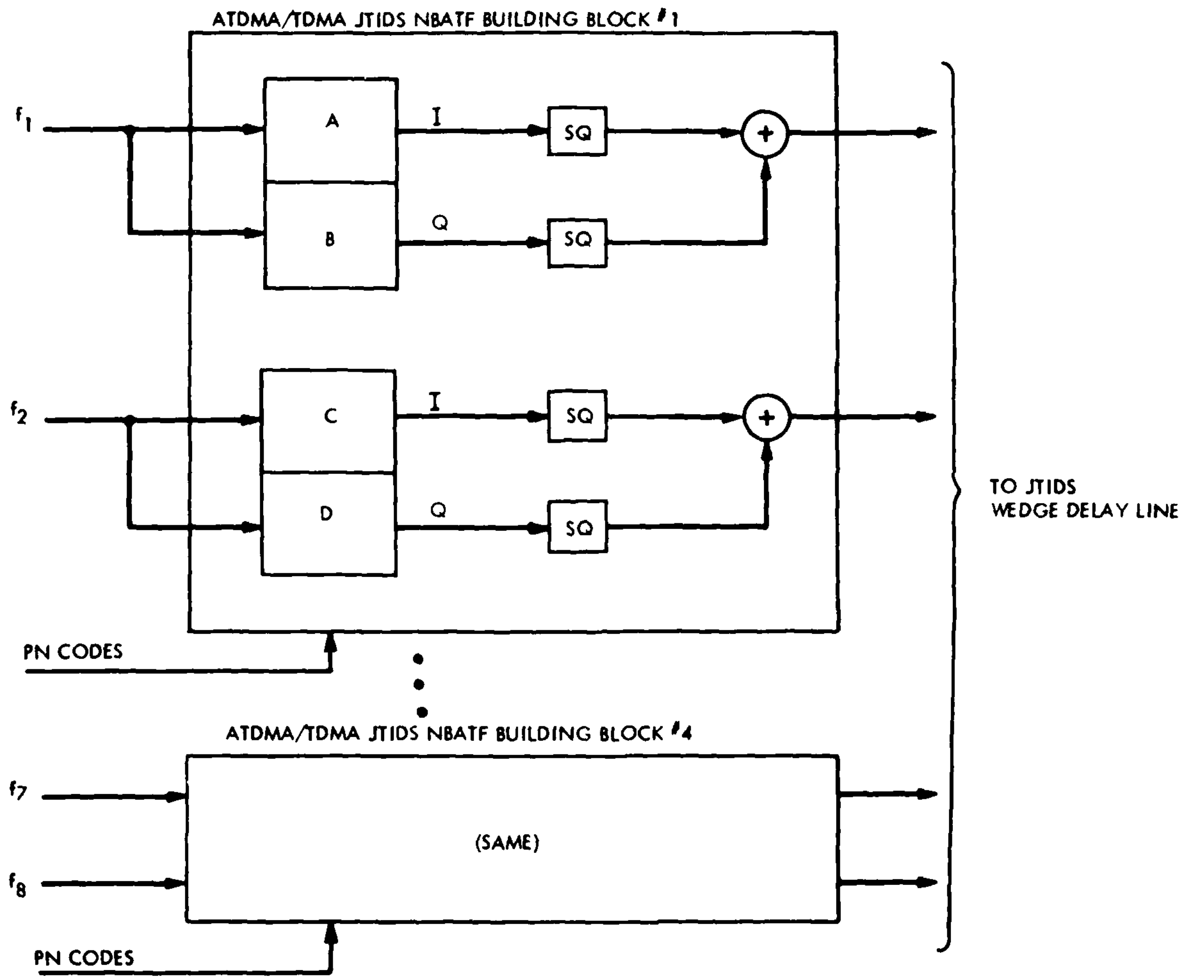


Figure 23. NBATF configuration, ATDMA/TDMA JTIDS sync

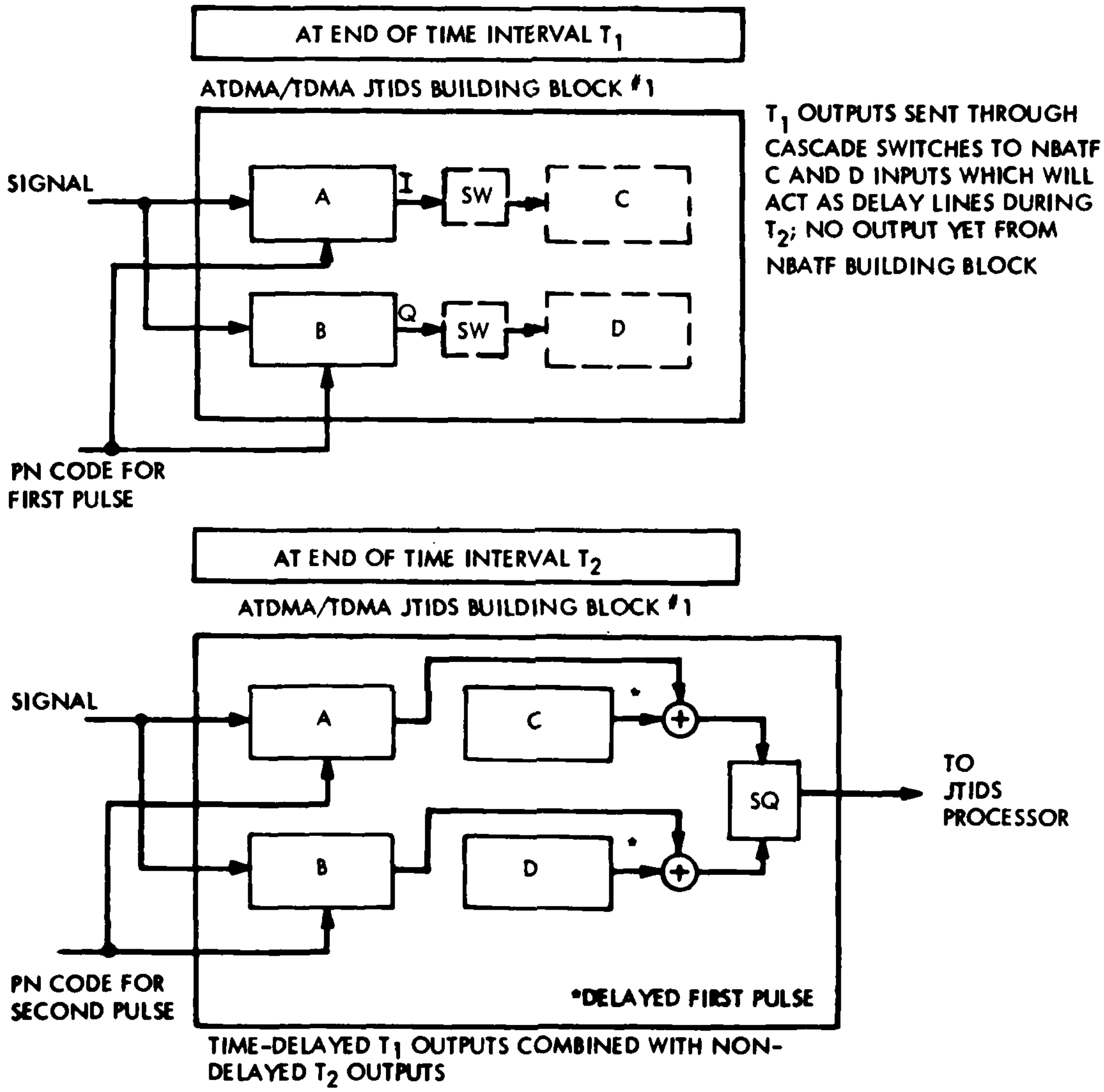


Figure 24. NBATF configuration, ATDMA/TDMA data mode

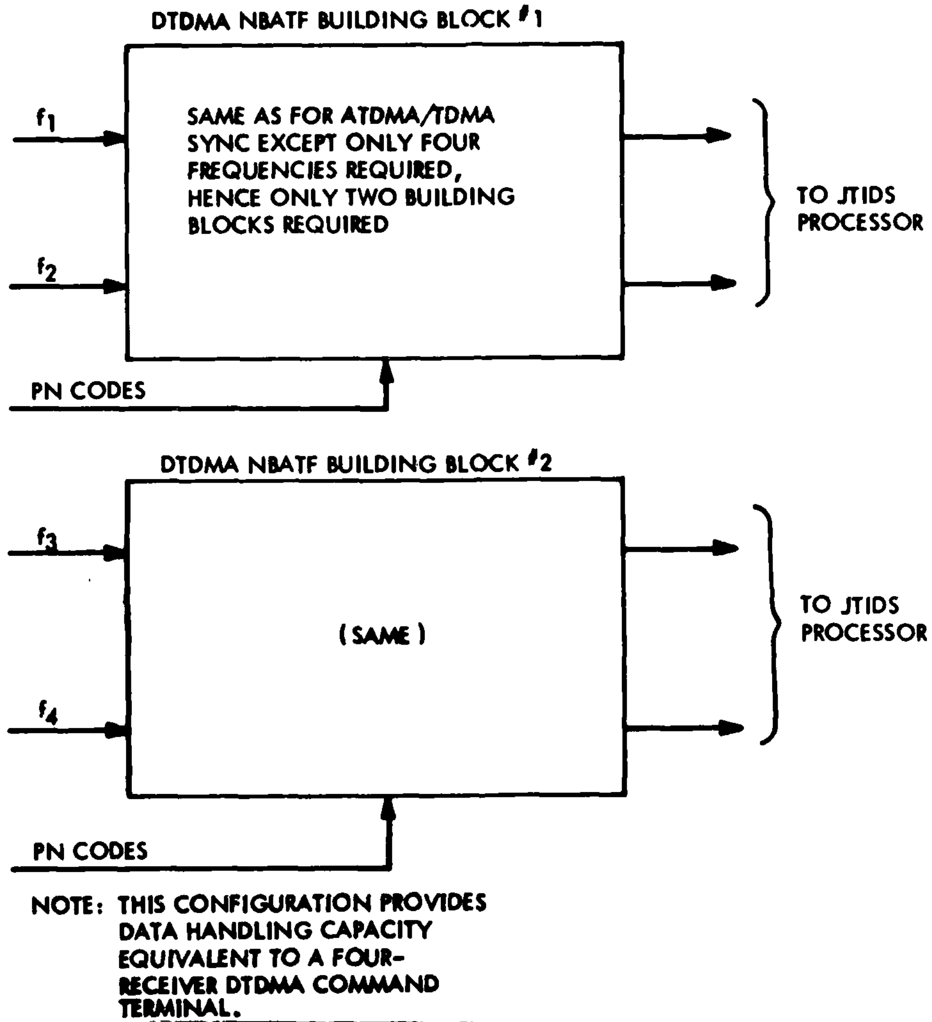
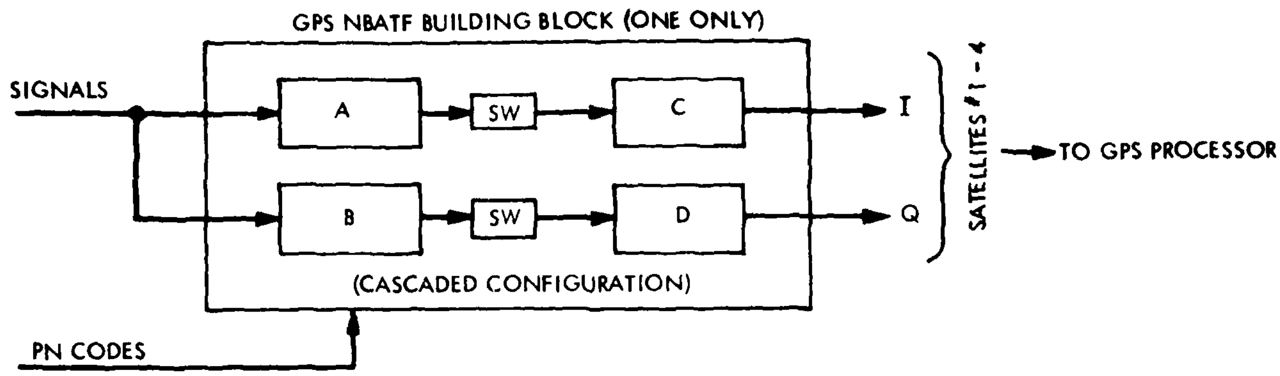


Figure 25. NBATF configuration for JTIDS DTDMA, both sync and data modes



NOTES: (1) CLOCK = 10.23 x n FOR GPS PROCESSING

(2) PN REFERENCE CODES WILL BE AGILELY CYCLED TO PROVIDE SIGNAL PROCESSING CAPACITY EQUIVALENT TO FOUR CONVENTIONAL GPS CHANNELS.

Figure 26. NBATF configuration, GPS

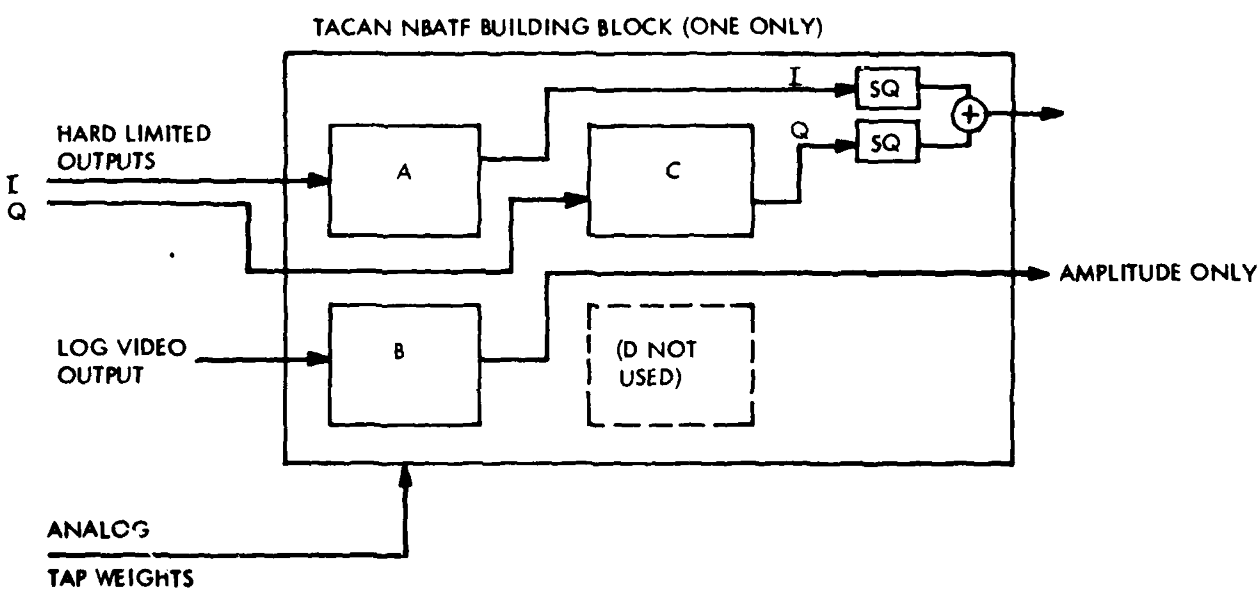


Figure 27. NBATF configuration, TACAN

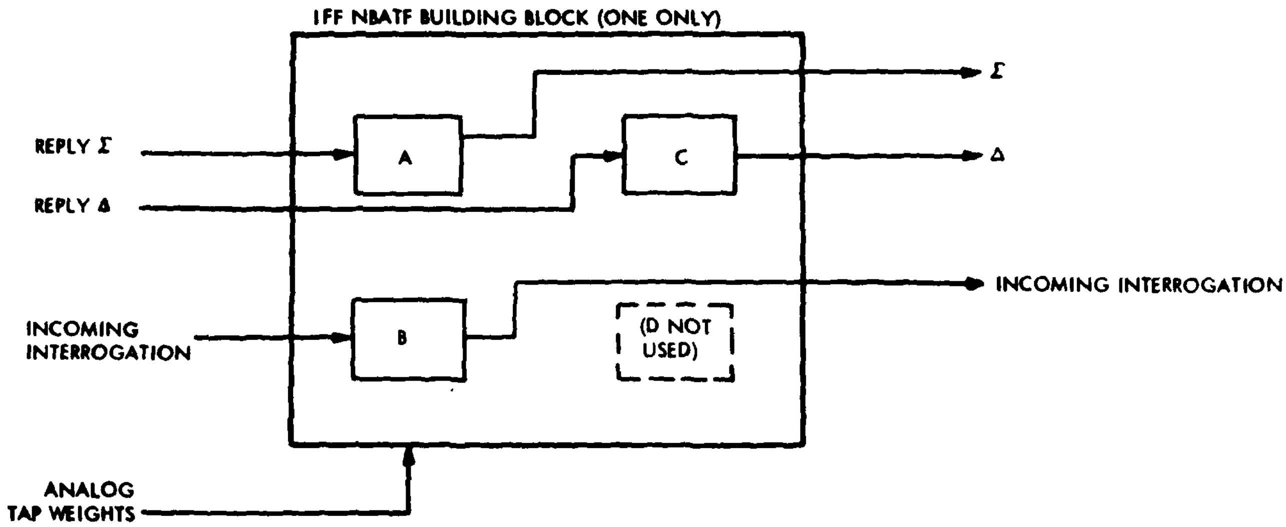


Figure 28. NBATF configuration, IFF

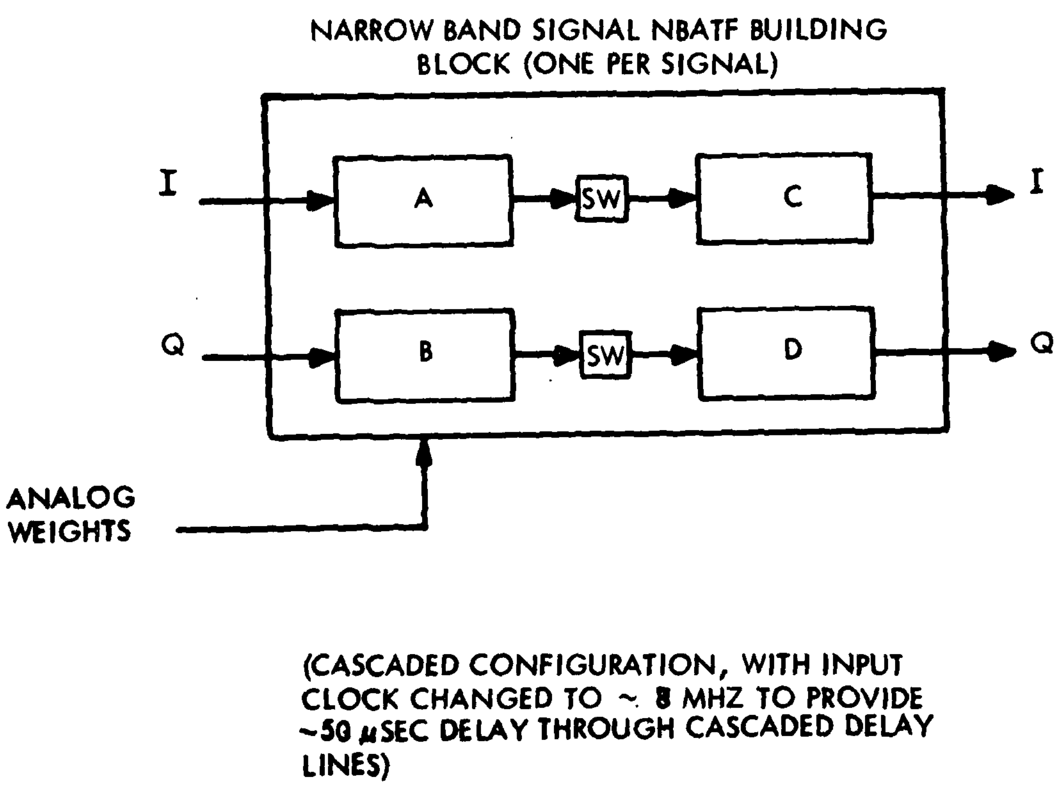


Figure 29. NBATF configuration, narrowband signals

2.4 DATA AND CONTROL PROCESSOR SUBSYSTEM

The Data and Control Processor Subsystem provides six main functions for MFBARS:

- system processing
- interface (via DAIS) with externally generated control commands
- internal control of the MFBARS subsystems, in response to the externally generated control commands
- processing, formatting and routing (via DAIS, to external aircraft systems) of digital data outputs from the Signal Processor Subsystem
- formatting and routing to appropriate modulation and transmitter circuitry of messages generated on-board the aircraft for MFBARS transmission
- control of the MFBARS BITE Subsystem

The subsystem consists of a dynamically reconfigurable multiprocessor array containing:

- multiple microprocessors
- modularized main memory (in which is stored all system operating programs and the system data base)
- internal and external I/O's
- an interconnection structure

The two main reasons for selecting a multiprocessor architecture are to provide for efficient partitioning of the total MFBARS computational work load and to provide a means for fail-soft reallocation of subsystem resources in the event of failure of any element of the subsystem. Figure 30 shows the basic architecture of the Data and Control Processor Subsystem.

Specific details of the subsystem have not yet been defined. This is because there are a large number of optional multiprocessor architectures to be reviewed and many MFBARS-unique requirements to be integrated into candidate multiprocessor architectures before the best approach can be determined. Completion of these efforts is beyond the funding resources of the current contract and will be accomplished in the next phase of the program. Nevertheless, some preliminary design decisions have been made. The following paragraphs present these preliminary design decisions.

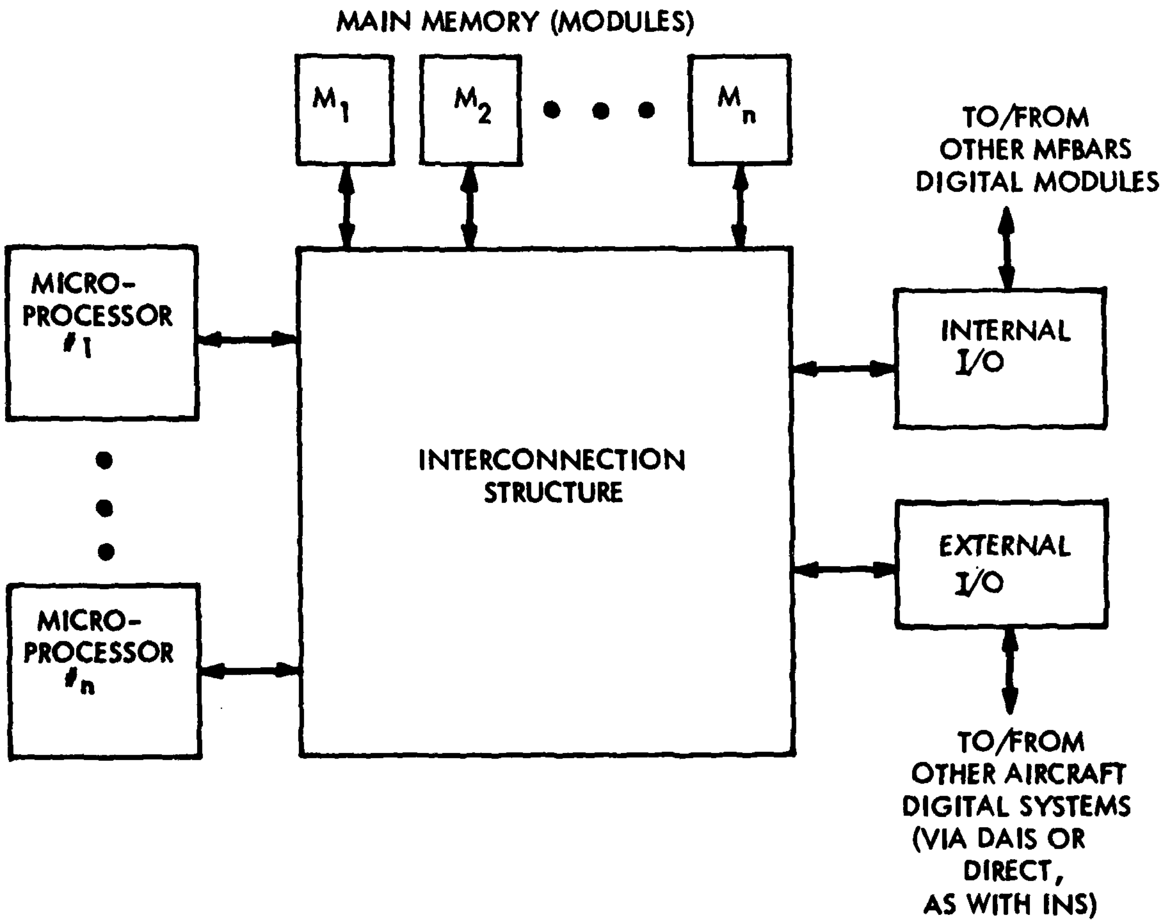


Figure 30. Data and control processor subsystem architecture

2.4.1 Architecture

The basic multiprocessor architecture will be an adaptation of a tested, proven military or commercial computer multiprocessor architecture (rather than a totally new architecture), to take advantage of existing designs to reduce risk and minimize development costs. There are a number of tested, proven candidates to choose from. Although the hardware aspects of the MFBARS implementation will be quite different, the proven machines contain applicable functional designs in the areas of:

- operating system software
- memory partioning and access techniques
- workload allocation
- failure sensing techniques
- reconfiguration techniques

Working from a proven functional design base will provide a low risk approach to this aspect of the MFBARS design.

2.4.2 Microprocessors

The subsystem will contain an estimated 3 or 4 advanced (1985-era) microprocessors. This projection is based on the following considerations:

(1) Today's typical militarized microprocessor has an effective throughput rate of up to about 1 MOPS.

(2) Processor technology has been widely projected to continue to grow at about 30 percent per year, in terms of effective throughput rate; thus, by around 1985, a conservative extrapolation of typical processor throughput capability would be almost 4 MOPS per microprocessor. VHSIC technology is expected to apply to this projected growth.

(3) From section 2.4.6, it is seen that MFBARS processing requirements are estimated to be about 8 MOPS (including a 30 percent margin for growth).

(4) Thus, about two 1985-era processors would be required to handle the basic projected MFBARS processing workload.

(5) An additional one or two processors may be added for redundancy for system reliability and for further functional growth margin.

(6) Thus, either 3 or 4 1985-era microprocessors are projected for MFBARS.

2.4.3 Main Memory

The subsystem will contain a modularized main memory, in which all system operating programs and the system data will be stored. The main memory will be partitioned into several memory modules. This will permit minimization of contention problems and will facilitate load leveling. There will be redundant memory for critical system functions and elements of the data base.

2.4.4 I/O's (Input/Output Devices)

There will be at least two I/O's in the subsystem, one for internal MFBARS digital interfaces and the other for all external interfaces between MFBARS and other aircraft digital systems (either via DAIS or directly, as in the case of INS). The I/O's may or may not be subdivided. Further study and tradeoff analysis is required before this decision can be made.

2.4.5 Interconnection Structure

Selection of the interconnection structure, which ties together the processors, the memory modules, and the I/O's, is the most complex design issue of the subsystem. There are three basic generic architectural approaches:

- common bus
- crossbar switch
- multi-port memory

The common bus has the advantage of simplicity of design and ease of expansion (up to some limit) for adding additional processors, memory or I/O devices. It is a relatively inexpensive and highly reliable approach. All processors would have access, through the common bus, to all main memory modules, which would facilitate load sharing and reconfiguration in the event of processor failure. The main disadvantage of the common bus approach is throughput limitations, due to contention. Also, even though highly reliable, bus failure of a common bus would cause total system failure.

The second generic approach (typified by C.mmp) is crossbar switching, in which every processor has access, via crossbar connections, to every global memory module. In this configuration, each processor can have its own local memory and dedicated I/O. The main advantage is more rapid access to the data base and the system operating programs. Also, contention is minimized, due to local memory and I/O. The

main disadvantages are system availability limitations, and difficulty in load sharing and reconfigurability because of the use of dedicated I/O's and dedicated local memories. Also, the crossbar connection hardware is expensive (currently), although 1985-era technological advances should lessen this disadvantage.

Multi-port memory solutions include a number of optional system approaches which increase the interconnection paths beyond the single path of a common bus structure without going to the extreme of complete crossbar interconnection between all processors and all memory modules. (This is the most frequent implementation used by mainframe manufacturers.) Advantages of all of these approaches include: increased overall subsystem reliability and reduction of contention problems due to the multiple bus paths; and ease of expandability.

The design complexity of the interconnection structure requires considerable further study and tradeoff analysis, to be accomplished in the next phase of the program.

2.4.6 Software*

All system operating software for MFBARS is stored in main memory of the Data and Control Processor Subsystem. A preliminary estimate of MFBARS software is given in Table 7. Detailed software definitions will be part of the next phase of the program.

2.5 BITE SUBSYSTEM

The BITE Subsystem is a major subsystem of the selected MFBARS system architecture. It contains both analog and digital test signal generators and analog and digital monitoring and evaluation circuitry to maintain a constant check on system health. It is under control of the Data and Control Processor Subsystem for normal automatic, periodic system checkout. Also, operator initiated action can activate BITE checkout routines for fault isolation of known or suspected out-of-limit performance. Working in conjunction with the Data and Control Processor Subsystem, detected failures can be bypassed or minimized by reconfiguration of the system. Memory elements within the BITE subsystem will provide a record of detected failures to aid post-flight system maintenance.

*Since software will be stored in (depot level replaceable) ROM's, it could more precisely be referred to as "firmware", but the more generic term "software" is used in this report, for convenience.

TABLE 7. SOFTWARE REQUIREMENTS (PRELIMINARY ESTIMATE)

	KOPS	Memory (Bytes)	Comments
1. Multiprocessor Operating System	850	40K	Multiprocessor Control, I/O Control, Resource Management, etc.
2. Application Programs			
JTIDS	1400	256K	DTDMA/TDMA
GPS	870	46K	Draper Labs projection
SEEK TALK	480	30K	Estimate
AFSATCOM	460	50K	Estimate
Nav	470	60K	
Comm	400	20K	
Data Base	-	256K	
3. Support Programs	1100	60K	AGC, math routines, etc.
Subtotal	6030	818K	
4. Growth Margin	1810	245K	30% (typical design margin)
Total	7840	1063K	

$$\text{Estimated* Instructions} \approx \frac{\text{Total Bytes - Data Base}}{2.4}$$

$$\approx \frac{1063 - 256}{2.4} K = 336.25K$$

*Based on JTIDS experience of average instruction length of 2.4 bytes/instruction

Analog and RF circuitry will be checked by means of test tone generators, receive and transmit signal strength measurements, and VSWR measurements. Digital circuitry will be checked by means of digital test words, as well as monitoring of parity bits and other digital checks built into message structures.

The special purpose processors in the Signal Processing Subsystem each have built-in digital test words and logic checks which enable self-test during normal operation and automatic fault indication reporting when a fault is detected.

The Data and Control Processor Subsystem has built-in test sequences for self monitoring and checkout of digital command and data flow between itself and other MFBARS subsystems and external aircraft digital systems (e.g. DAIS bus interface).

3. INTEGRATED NAVIGATION CONCEPTS

During the basic MFBARS study, the Government asked ITTAV to conduct a preliminary investigation of the feasibility of an optional higher level of system integration; namely, integration of MFBARS navigation signals with each other and with the on-board inertial navigation system (INS). Two concepts were explored:

- integration of GPS and JTIDS signal processing
- integration of GPS/JTIDS/INS signal processing

Preliminary results of the integrated navigation function study task were promising. Both hardware integration opportunities and operational benefits were identified. However, more detailed analysis is required to determine cost-performance effectiveness across the entire user community. If cost effective, an integrated navigation function could either be merged into the basic MFBARS program at this time or could follow as a subsequent program task.

GPS, JTIDS, and the INS all make use of similar navigation computations, all using Kalman filtering techniques. An integrated set of navigation algorithms, with common Kalman filtering, could lead to savings in navigation processor hardware and inertial system and aircraft interfaces. Figure 31 shows a top level block diagram of integrated GPS/JTIDS navigation hardware.

3.1 OPERATIONAL BENEFITS TO JTIDS USERS

The greatest potential operational benefit to JTIDS (of an integrated navigation function) would be the ability to utilize GPS inherent higher accuracy timing and geodetic position location capability. GPS provides high accuracy, receive-only, position location and timing information, in one common world-wide geodetic coordinate reference grid, for all GPS users. In contrast, JTIDS provides relative navigation (relnav) capability by means of two-way position location message interchanges between participants in any given JTIDS network. Each JTIDS network establishes its own independent navigation reference grid and time reference.

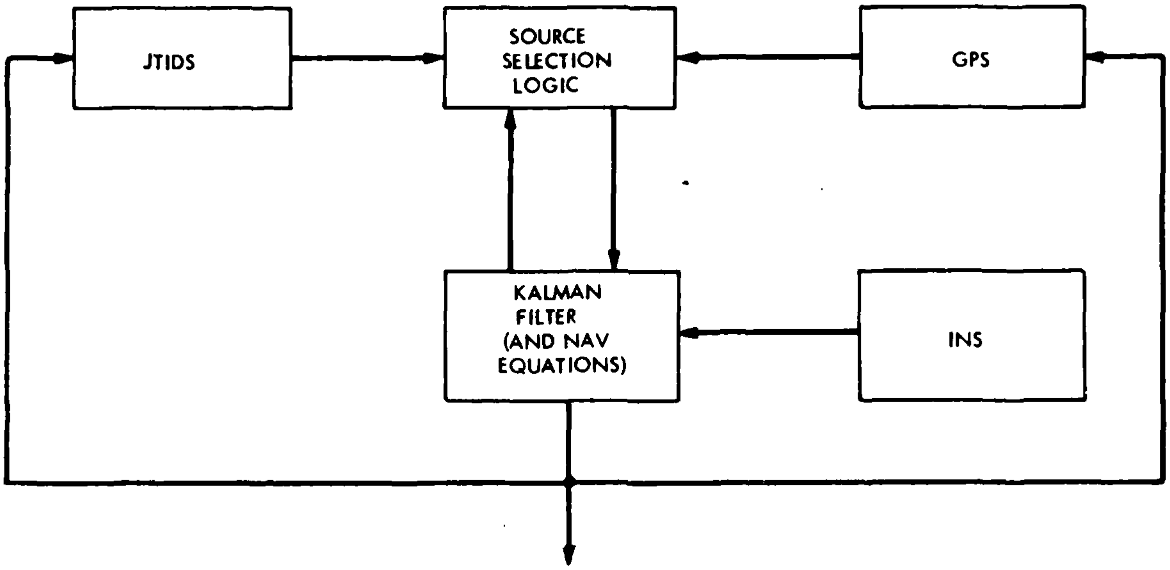


Figure 31. Fully integrated system structure GPS/JTIDS/INS

Geodetic benchmarks are required (for each JTIDS network) to permit position location repeatability and exchange of target data and other ground-related data between cooperating aircraft and between aircraft and air tactical control centers. Use of GPS common worldwide geodetic coordinates would simplify establishing common geodetic benchmarks for JTIDS networks.

Furthermore, the total mix of navigation data available to the Kalman filter from an integrated GPS/JTIDS would permit rapid navigation signal reacquisition not possible with independent systems.

3.2 OPERATIONAL BENEFITS TO GPS USERS

The primary operational benefit to GPS users (of an integrated navigation function) would come about when a GPS user could not directly receive a sufficient number of GPS satellite signals for accurate GPS position location computations. At least four GPS satellite signals must be received to complete each computation. Furthermore, the four satellites must have adequate angular separation, for geometric reasons. Under many foreseeable circumstances (including deliberate enemy jamming, atmospheric attenuation anomalies, non-optimum or incomplete GPS constellation configurations, and other factors), a GPS-user may receive some, but not all, of the necessary GPS signals required for accurate position location computations. In those cases, if the missing signal(s) could be obtained by other GPS-equipped platforms at locations sufficiently different to receive the missing signals, and if the missing information could be fulfilled using the JTIDS relative grid and/or could be transferred via JTIDS messages, then each GPS user could complete its own GPS computations, even though some of the inputs would be received indirectly. Importantly, during periods of GPS signal loss, the JTIDS timing data, properly filtered by the Kalman algorithms, could maintain close synchronism with the virtual GPS signal code. Thus, when the GPS signal returned to a detectable level, almost immediate reacquisition would be possible.

4. RECOMMENDED PROGRAM PLAN

With the completion of MFBARS Phases I and II, the program is ready to enter two parallel follow-on phases, Concept Validation Tasks and Support (or Operational Impact) Tasks. Concept Validation Tasks are those which will reduce program risk by demonstrating feasibility of critical system concepts before proceeding to ADM. Support (or Operational Impact) Tasks are those tasks which involve interactions between MFBARS and other systems, deployment and support interactions, life cycle cost, etc. Upon completion of both of these groups of tasks, the program can proceed to Concept Refinement and then to ADM with minimum risk. Figure 32 shows the general interrelationship of these groups of follow-on program tasks.

Figure 33 shows a more detailed program plan, with major tasks identified. (The tasks are numbered to tie in with the top level grouping of Figure 32).

Tasks 2.1 through 2.14 represent a logical and progressive demonstration of validity of the most innovative aspects of the system concept, starting with development and demonstration of an innovative new technology device, the wideband agile transversal filter (WBATF) (tasks 2.1 through 2.5). As shown, there is a high degree of interaction between tasks 2.3 and 2.4, the device development and the parallel development of demonstration hardware and software. Upon completion of development of both the device and the demonstration hardware/software, task 2.5 demonstrates and evaluates WBATF signal processing and integrated adaptive antenna processing.

A similar grouping of tasks (2.6 through 2.10) provides for device development and concept demonstration of narrowband agile transversal filter (NBATF) signal processing, another critical system function. There are similar interactive relationships between some of the tasks, as in the case for the WBATF.

Upon completion of WBATF and NBATF demonstration and evaluation, results can be used for refinement of device parameters (task 2.11) to allow progression from prototype device status to more refined devices (task 2.12) for the ADM phase of the program.

Tasks 2.13 and 2.14 provide refinement of other design areas not completed in depth in MFBARS Phase II.

Upon completion of these four areas of group 2.0 tasks (WBATF, NBATF, control processor, and BITE/fail-soft reconfiguration capability), the major innovative aspects

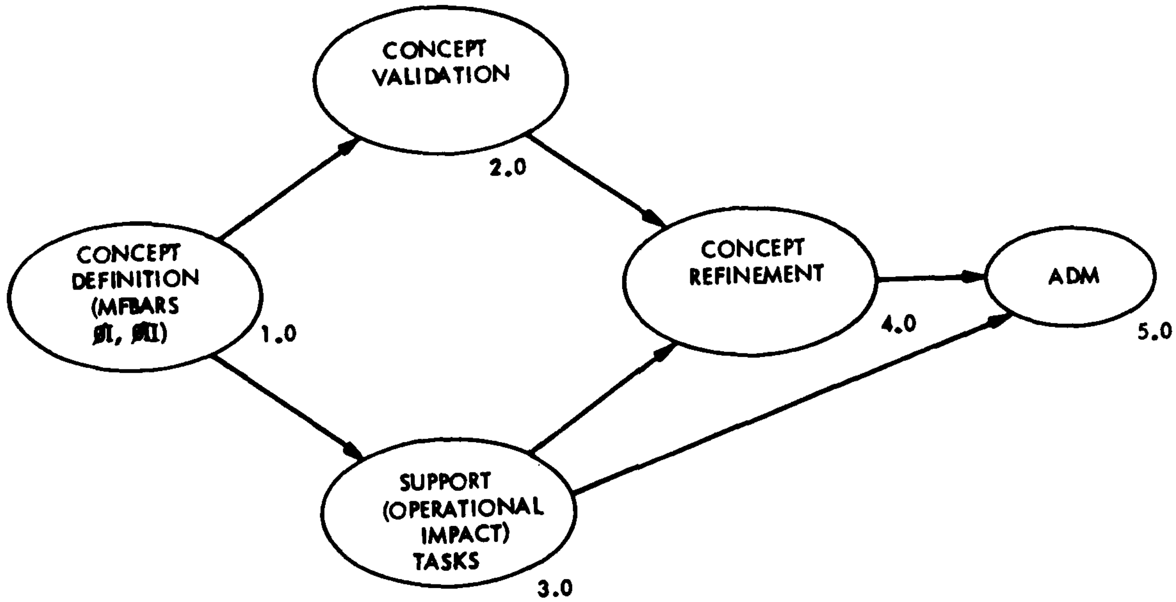
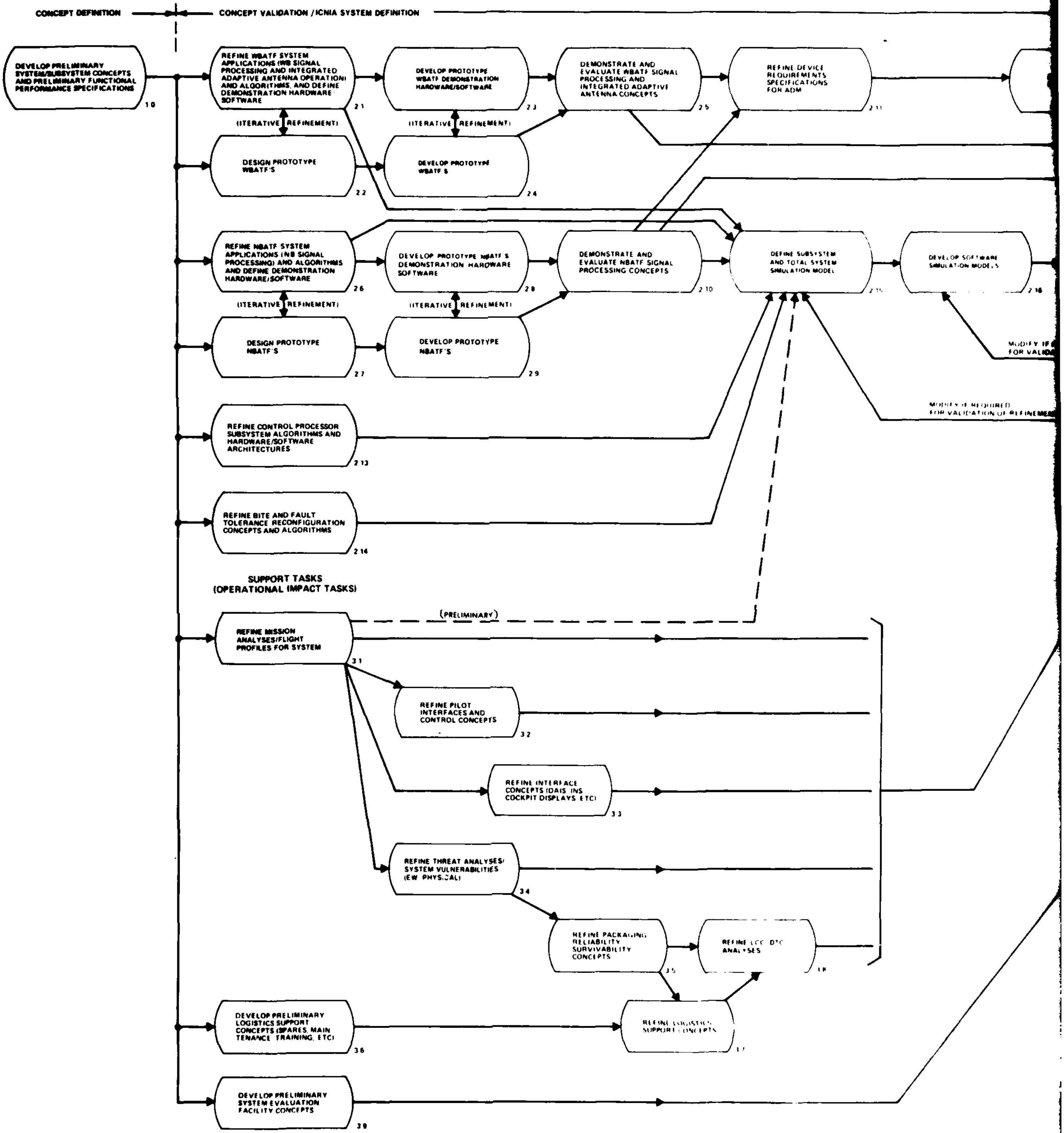


Figure 32. Program flow chart



CONCEPT DEFINITION
CONCEPT VALIDATION / ICNIA SYSTEM DEFINITION
DEVELOP PRELIMINARY SYSTEM/SUBSYSTEM CONCEPTS AND PRELIMINARY FUNCTIONAL PERFORMANCE SPECIFICATIONS 1.0
REFINE WBATF SYSTEM APPLICATIONS (WB SIGNAL PROCESSING AND INTEGRATED ADAPTIVE ANTENNA OPERATION) AND ALGORITHMS, AND DEFINE DEMONSTRATION HARDWARE/SOFTWARE 2.1
DESIGN PROTOTYPE WBATF'S 2.2
DEVELOP PROTOTYPE WBATF DEMONSTRATION HARDWARE/SOFTWARE 2.3
DEVELOP PROTOTYPE WBATF'S 2.4
DEMONSTRATE AND EVALUATE WBATF SIGNAL PROCESSING AND INTEGRATED ADAPTIVE ANTENNA CONCEPTS 2.5
REFINE DEVICE REQUIREMENTS SPECIFICATIONS FOR ADM 2.11
(ITERATIVE REFINEMENT)
REFINE NBATF SYSTEM APPLICATIONS (NB SIGNAL PROCESSING) AND ALGORITHMS AND DEFINE DEMONSTRATION HARDWARE/SOFTWARE 2.6
DESIGN PROTOTYPE NBATF'S 2.7
DEVELOP PROTOTYPE NBATF'S DEMONSTRATION HARDWARE SOFTWARE 2.8
DEVELOP PROTOTYPE NBATF'S 2.9
DEMONSTRATE AND EVALUATE NBATF SIGNAL PROCESSING CONCEPTS 2.10
DEFINE SUBSYSTEM AND TOTAL SYSTEM SIMULATION MODEL
DEVELOP SOFTWARE SIMULATION MODELS 2.16
MODIFY IF REQUIRED FOR VALIDATION OF REFINEMENTS
REFINE CONTROL PROCESSOR SUBSYSTEM ALGORITHMS AND HARDWARE/SOFTWARE ARCHITECTURES 2.13
REFINE BITE AND FAULT TOLERANCE RECONFIGURATION CONCEPTS AND ALGORITHMS 2.14
SUPPORT TASKS (OPERATIONAL IMPACT TASKS)
(PRELIMINARY)
REFINE MISSION ANALYSES/FLIGHT PROFILES FOR SYSTEM 3.1
REFINE PILOT INTERFACES AND CONTROL CONCEPTS 3.2
REFINE INTERFACE CONCEPTS (DAIS, INS, COCKPIT DISPLAYS, ETC) 3.3
REFINE THREAT ANALYSES/SYSTEM VULNERABILITIES (EW, PHYSICAL) 3.4
REFINE PACKAGING RELIABILITY SURVIVABILITY CONCEPTS 3.5
REFINE LCC, DTC ANALYSES
DEVELOP PRELIMINARY LOGISTICS SUPPORT CONCEPTS (SPARES, MAINTENANCE, TRAINING, ETC) 3.6
REFINE LOGISTICS SUPPORT CONCEPTS 3.7
DEVELOP PRELIMINARY SYSTEM EVALUATION FACILITY CONCEPTS 3.9

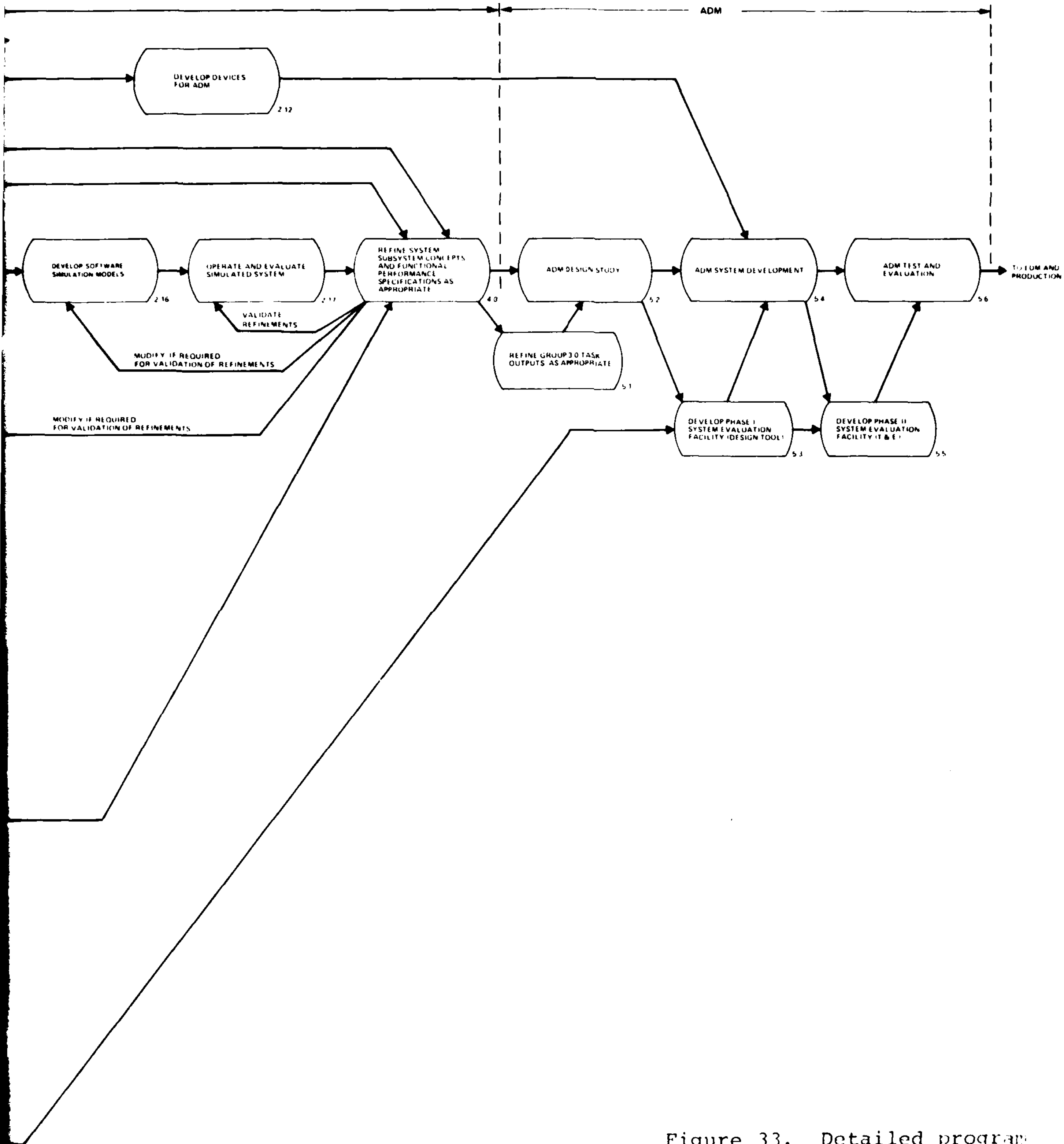


Figure 33. Detailed program flow chart

of the system will have been individually demonstrated and evaluated. The next step will be to validate their interactions with each other and with other less innovative aspects of the system design concept. At this point in system validation, a simulation model is the most practical means of demonstrating overall integrated system performance concepts. Tasks 2.15 through 2.17 involve development and operation of a system simulation model and evaluation of the integrated results. Note, that the model also utilizes inputs from the group 3.0 tasks, the support or operational impact tasks. The group 3.0 tasks provide inputs needed by the model in terms of realistic timelines, system signal loads, control and display time-sharing, pilot interactions, impact of external threats (EW and physical) which might interfere with system operation, etc. Without these group 3.0 inputs, system load could not be realistically simulated.

Group 3.0 tasks serve other purposes as well as providing inputs to the system simulation model. Tasks 3.1 through 3.3 represent refinements of other earlier data which provided rough mission constraints and requirements information for initial development of MFBARS system concepts. Now that a system concept has been developed, it is necessary to review the constraints and requirements information to make sure that the missions would still be performed the same way as originally defined or whether refinements may be appropriate. This could be considered a type of "sensitivity analysis" to validate that the resultant overall system capabilities are still well matched and balanced to the overall mission requirements. In addition, some inputs, such as pilot interfaces, need refinement which could not be done prior to availability of a specific system concept.

Task 3.4, in addition to providing an input to the system simulation model, also provides critical inputs to refinements of packaging, survivability, and reliability concepts for the system (task 3.5). These, in turn, provide needed inputs to tasks 3.7 and 3.8, which are refinements of logistics support concepts and life cycle cost and design to cost (LCC/DTC) analyses. Preliminary logistics concepts can be started (task 3.6) using basic system concept information, but refinement (task 3.7) requires packaging inputs from task 3.5.

Finally, among the support tasks is a very important task (3.9) which initiates definition of a System Evaluation Facility required to support ADM development and ADM test and evaluation. The multiple signals and complex

interactions the system must handle requires a System Evaluation Facility beyond any now available. Initial concepts must be started early to assure availability of the necessary facility at the proper time.

Completion of all group 2.0 and 3.0 tasks enables initiation of task 4.0, refinement of system/subsystem concepts and functional performance specifications, as appropriate. Although shown as only a single task in the program plan (plus feedback to earlier tasks), it could be a very significant task and may be broken into smaller subtasks later, depending upon the outcome of system simulations and task group 3.0 inputs. Also, although not shown on the diagram for reasons of clarity, many of the other task outputs may also influence task 4.0. As shown, significant changes are fed back to tasks 2.15 through 2.17, as required, to make sure refinements are validated before proceeding to ADM. Also, group 3.0 tasks will be refined as appropriate, although refinement details are not shown, for clarity.

When the system concepts have been refined and validated to the satisfaction of the Government, then the program can proceed to ADM with minimal risk. Only six ADM (group 5.0) tasks are shown on the program plan at this time. Each represents a significant program effort and could be subdivided into more detail later. The major relationships are evident, however, including input of task 2.12 refined ADM devices, which have been developed in parallel with other tasks. Upon completion of ADM (task 5.6), the program can proceed to EDM and subsequently to production.